

FOXCONN A75M02

FAB: 1.0

AMD FM1 APU + FCH HUDSON D2/D3 CHIPSET

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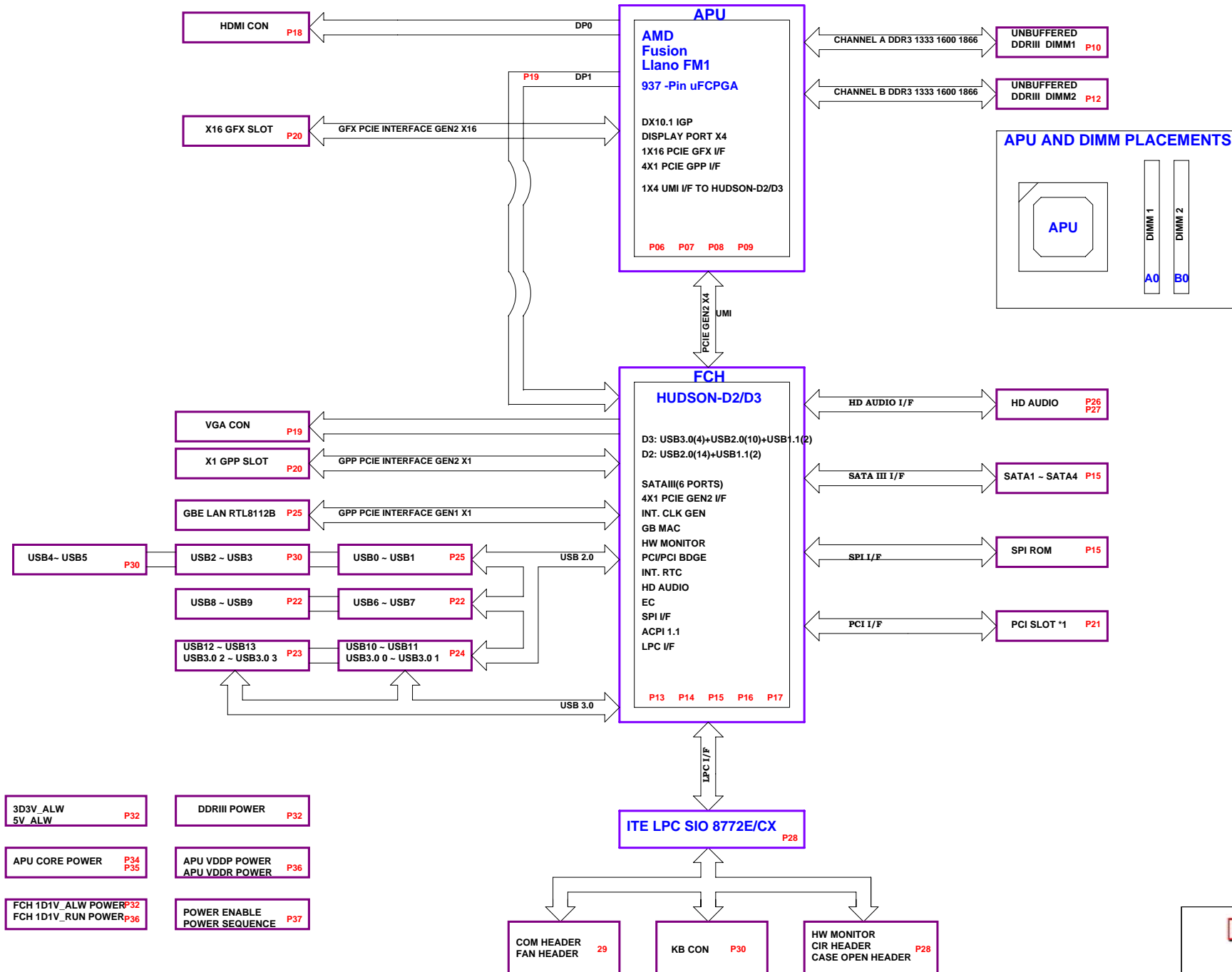
| | |
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| P03: POWER DELIVERY CHART | P23: USB3.0 FRONT HEADER |
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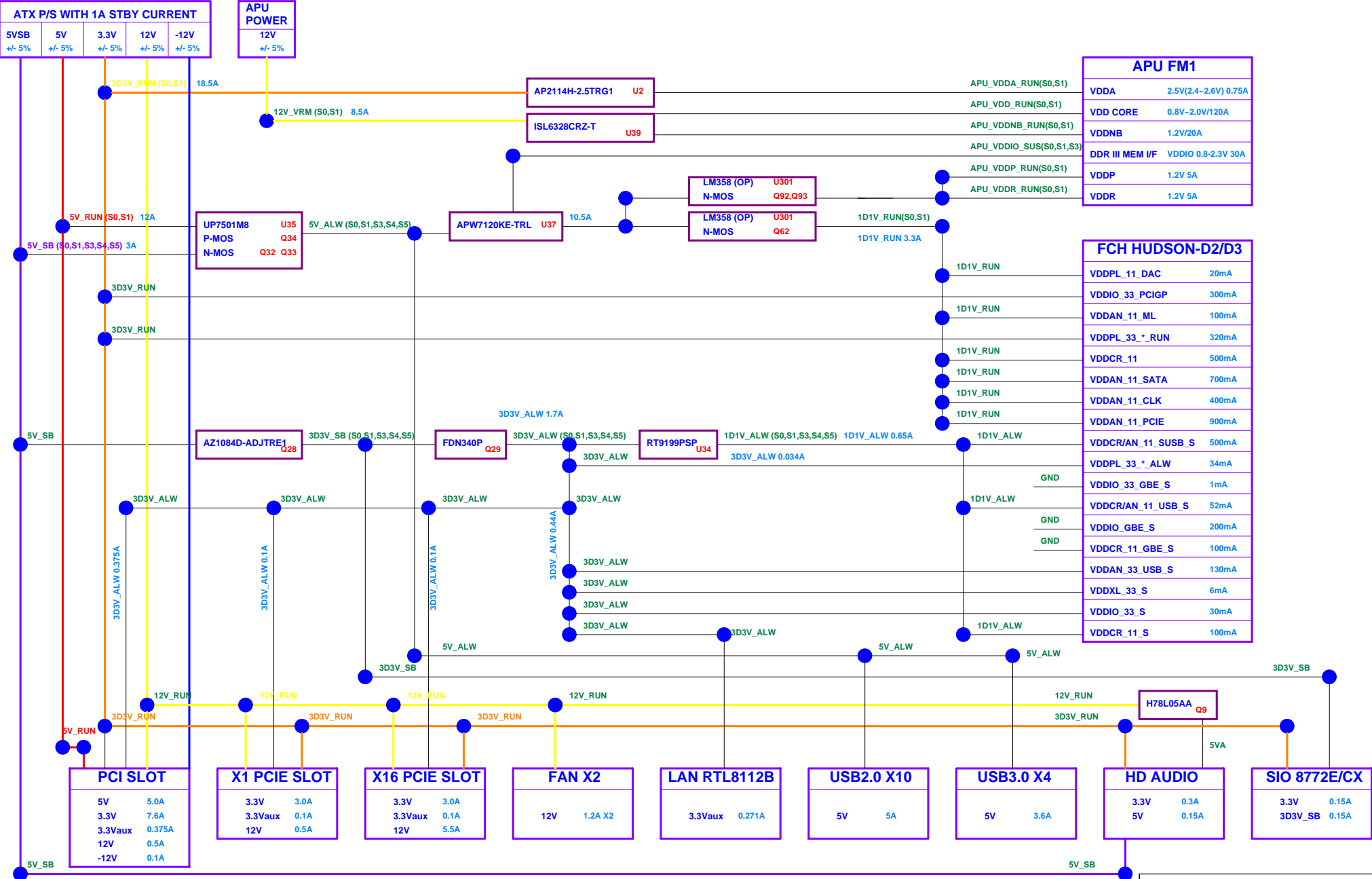
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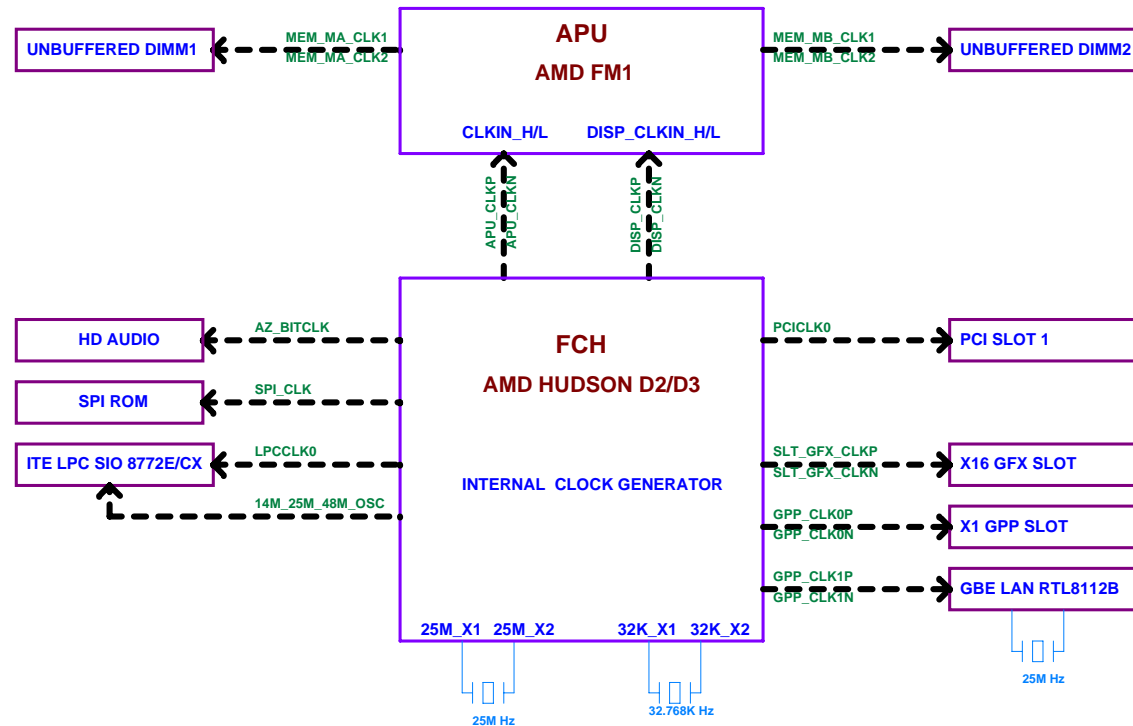
A75M02 BLOCK DIAGRAM



A75M02 POWER DELIVERY CHART



A75M02 INTERNAL CLOCK MODE



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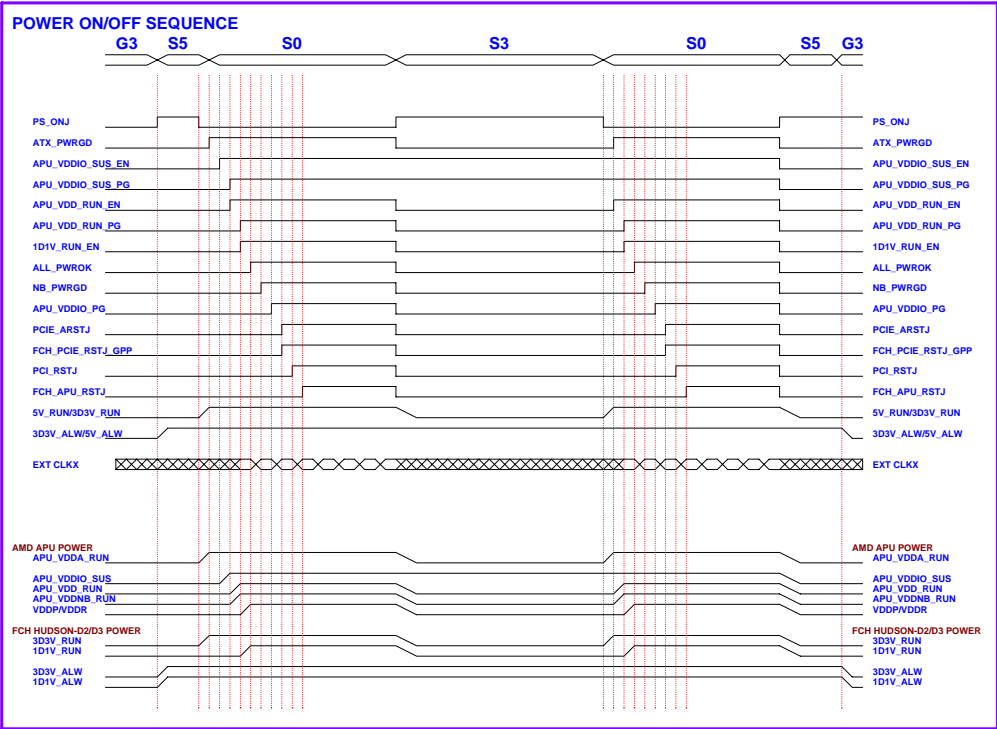
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| Title | | | |
| CLOCK DISTRIBUTION | | | |
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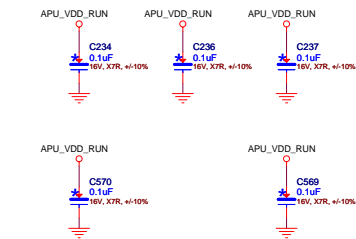
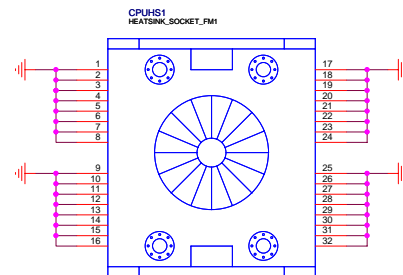
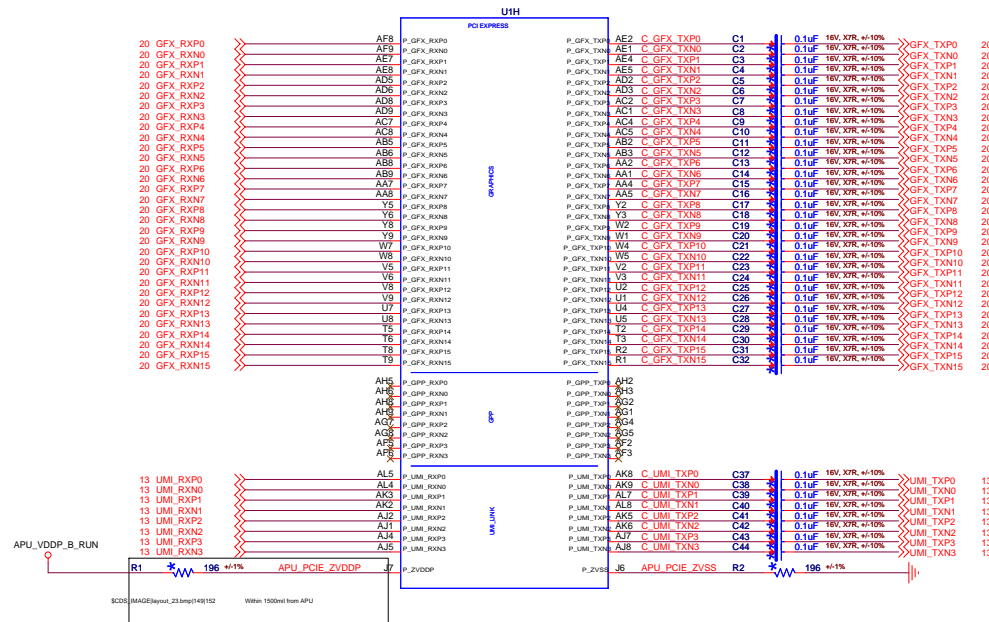
A75M02 MISC TABLES

| POWER RAIL | | S0 | S1 | S3 | S4 | S5 | POWER RAIL | | S0 | S1 | S3 | S4 | S5 |
|------------|-------|----|----|-----|-----|-----|---------------|--------|----|----|-----|-----|-----|
| 12V_RUN | +12V | ON | ON | OFF | OFF | OFF | 1D1V_RUN | +1.1V | ON | ON | OFF | OFF | OFF |
| 12V_VRM | +12V | ON | ON | OFF | OFF | OFF | APU_VDD_RUN | SVI | ON | ON | OFF | OFF | OFF |
| N_12V_RUN | -12V | ON | ON | OFF | OFF | OFF | APU_VDDNB_RUN | SVI | ON | ON | OFF | OFF | OFF |
| 5V_SB | +5V | ON | ON | ON | ON | ON | APU_VDDA_RUN | +2.5V | ON | ON | OFF | OFF | OFF |
| 3D3V_SB | +3.3V | ON | ON | ON | ON | ON | APU_VDDIO_SUS | +1.5V | ON | ON | ON | OFF | OFF |
| 5V_ALW | +5V | ON | ON | ON | ON | ON | APU_VTT_SUS | +0.75V | ON | ON | OFF | OFF | OFF |
| 3D3V_ALW | +3.3V | ON | ON | ON | ON | ON | APU_VDDR_RUN | +1.2V | ON | ON | OFF | OFF | OFF |
| A_VBAT | +3.0V | ON | ON | ON | ON | ON | APU_VDDP_RUN | +1.2V | ON | ON | OFF | OFF | OFF |
| 1D1V_ALW | +1.1V | ON | ON | ON | ON | ON | | | | | | | |
| 5V_RUN | +5V | ON | ON | OFF | OFF | OFF | | | | | | | |
| 3D3V_RUN | +3.3V | ON | ON | OFF | OFF | OFF | | | | | | | |
| 5VA | +5V | ON | ON | OFF | OFF | OFF | | | | | | | |

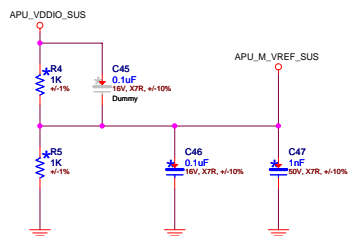
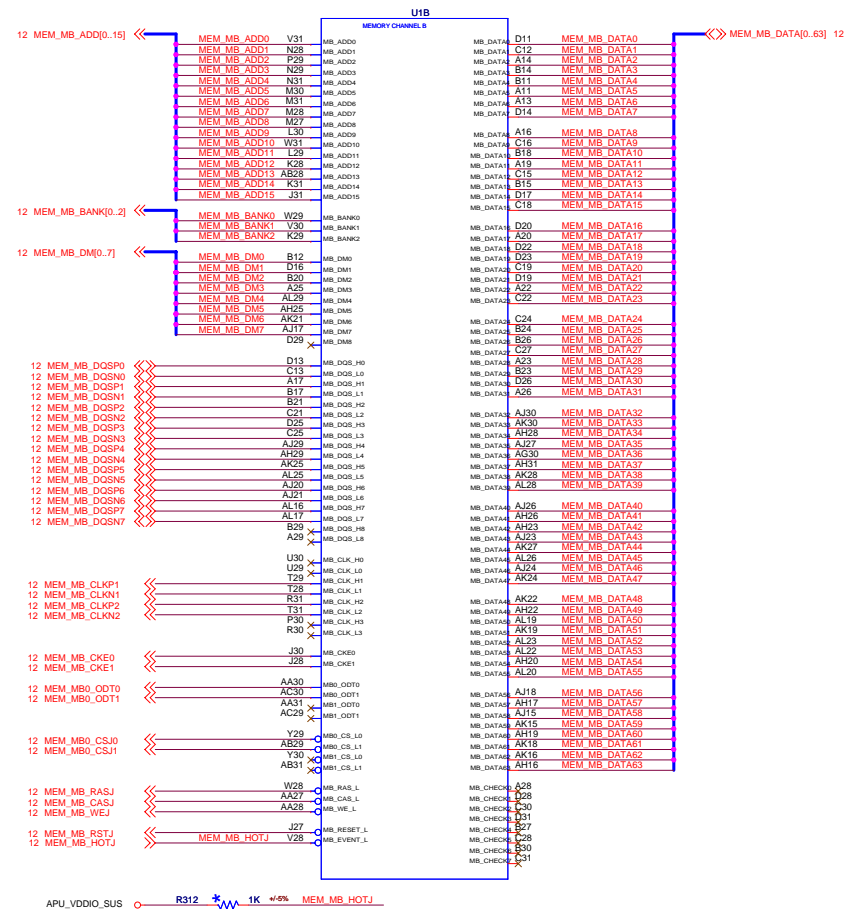
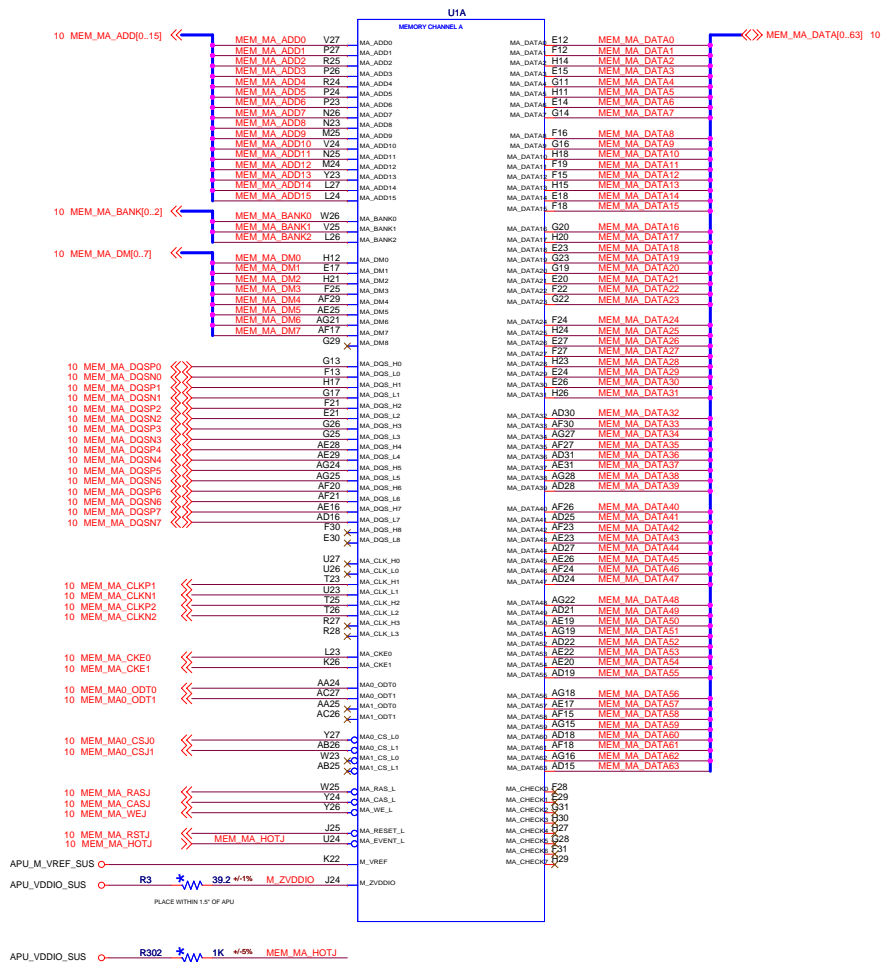
| RESET TABLE | | |
|-------------|-------------------|--------------------------------|
| SOURCE | SIGNAL NAME | LINKED DEVICES |
| FCH | PCIE_RST2J_GPP | GPP X1 SLOT/ LAN RTL8112B |
| | FCH_PCIE_RSTJ_GPP | GFX X16 SLOT |
| | PCIE_ARSTJ | LPC SIO 8772E/CX |
| | PCI_RSTJ | PCI SLOT 0 |
| | FCH_APU_RSTJ | APU |
| APU | A_HDA_RSTJ | HD AUDIO CODEC ALC662/VT1705CE |
| APU | MEM_MA_RSTJ | DIMM1 |
| APU | MEM_MB_RSTJ | DIMM2 |
| PWR BTN | MASTER_RSTJ | FCH |

| Explanation | |
|-------------|-------------------------|
| FCH | Fusion Controller Hub |
| UMI | Unified Media Interface |



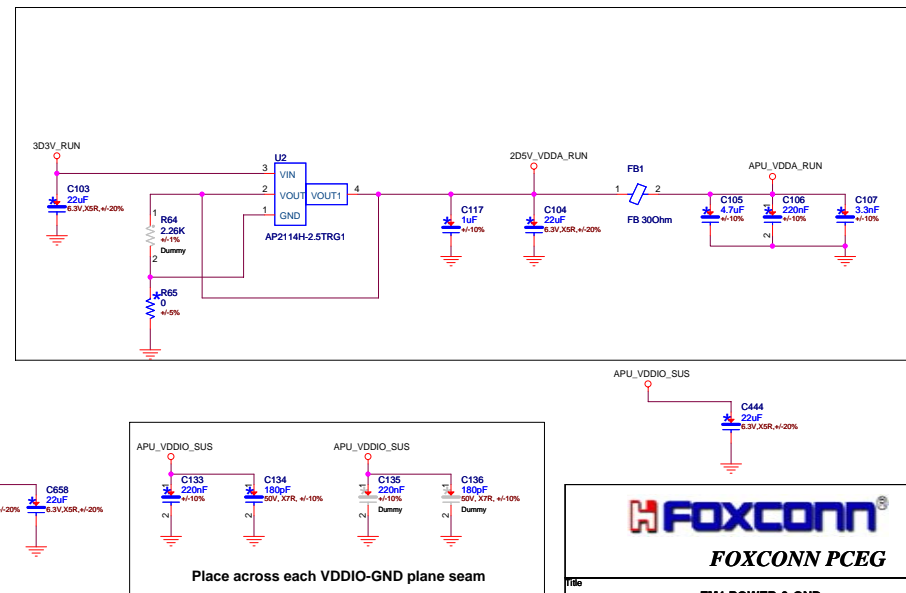
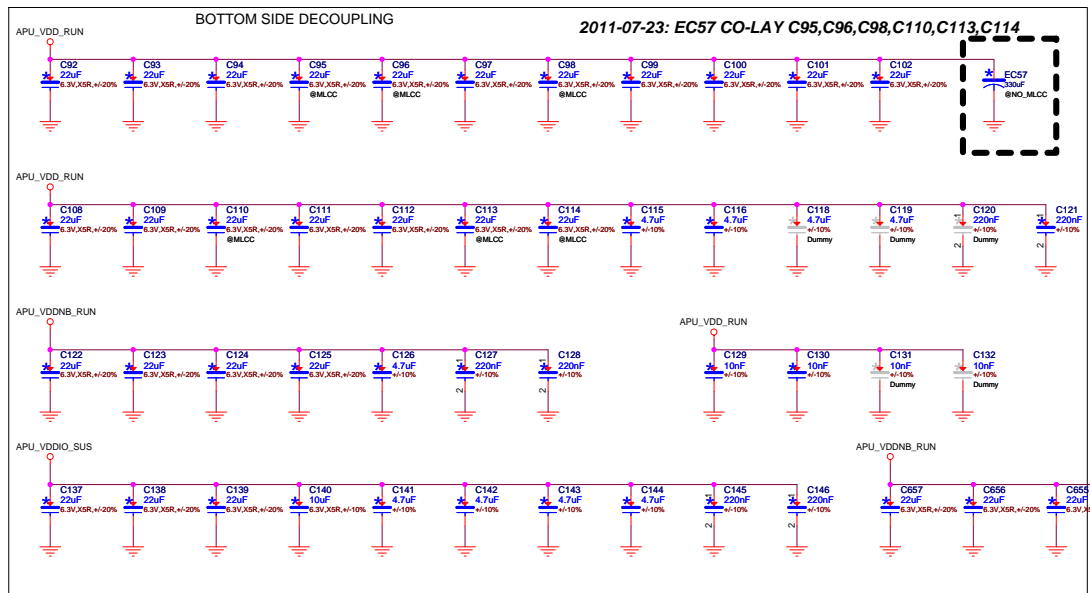
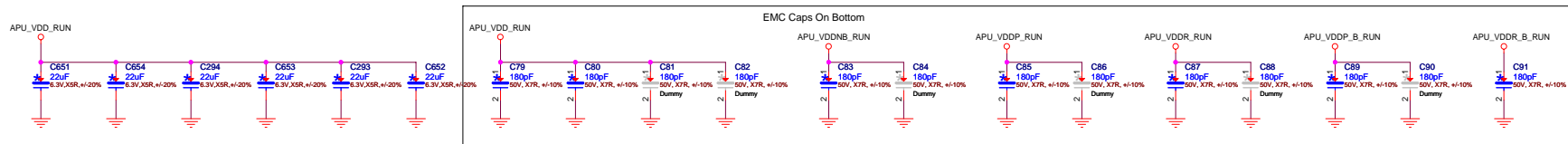
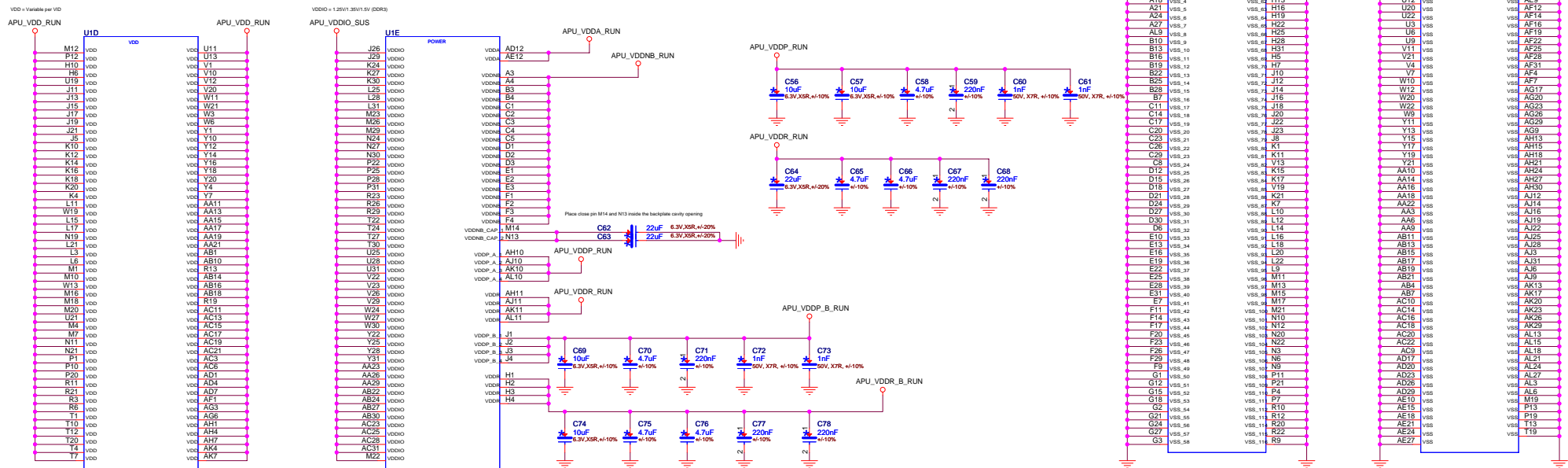


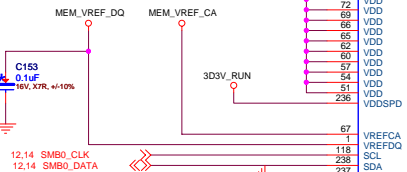
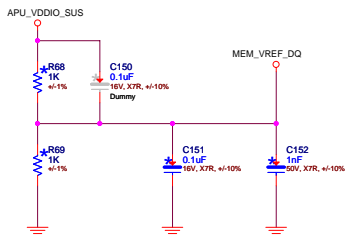
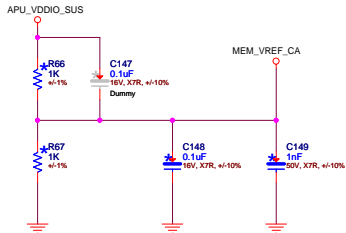
Place across each APU_VDD_RUN-GND plane seam



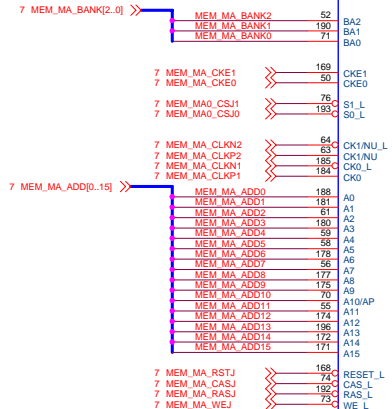
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PROCESSOR POWER AND GROUND

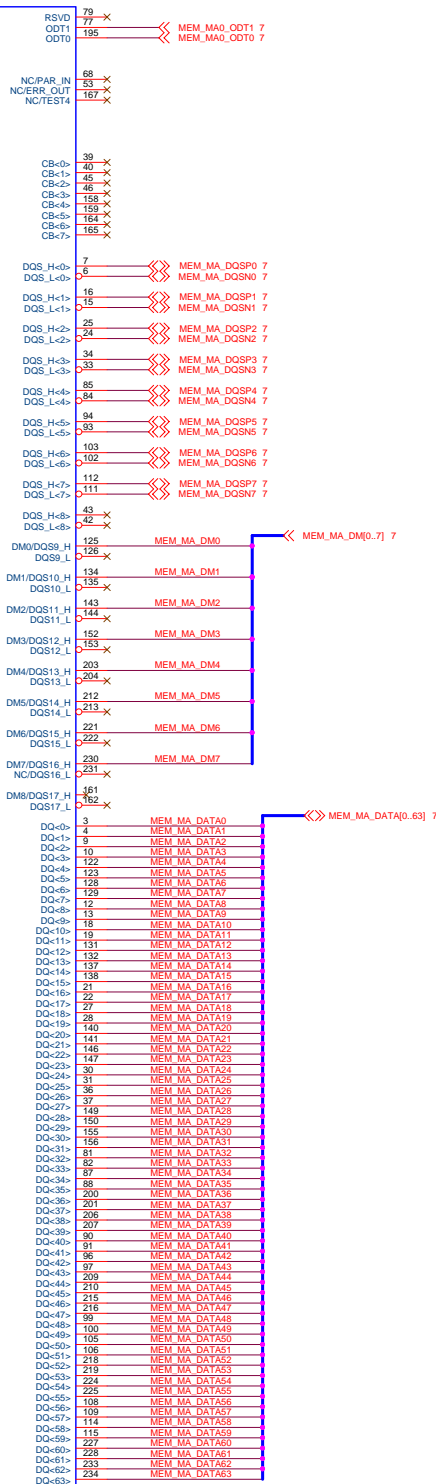




| SMBUS 0 | |
|---------|---------------------|
| Device | 8-bit Address (hex) |
| DIMMA0 | A0 |
| DIMMB0 | A2 |



DDR II

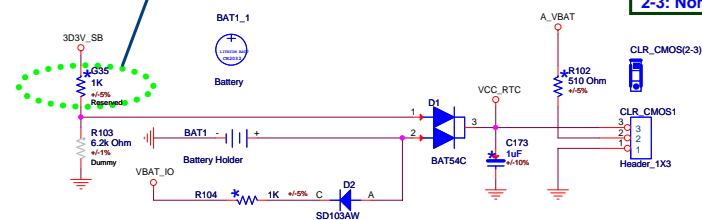
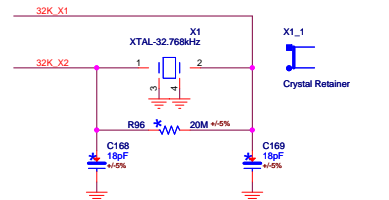




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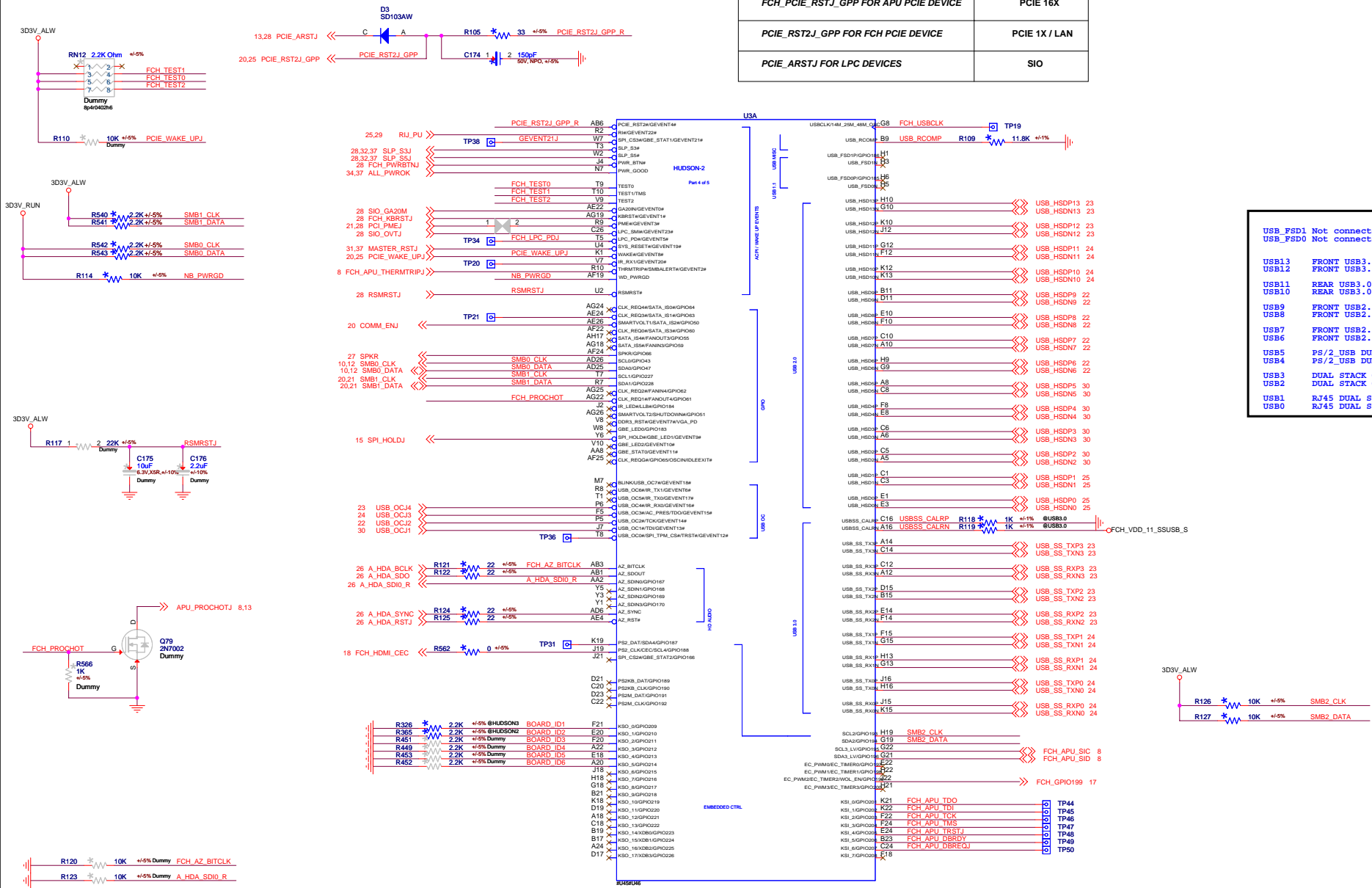
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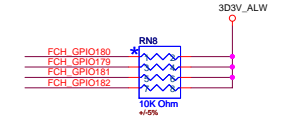
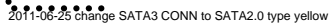


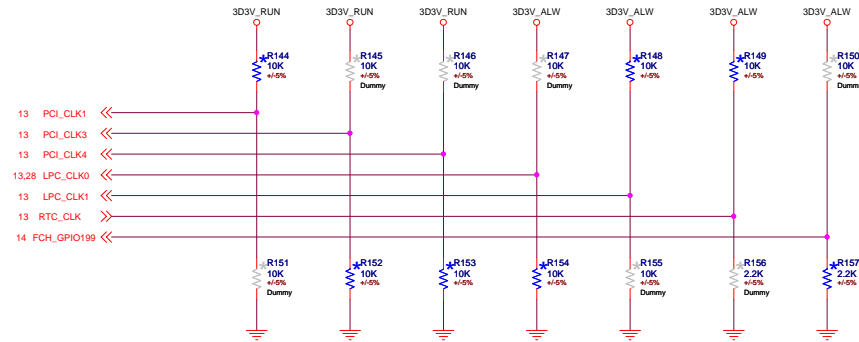
For A55MX

| | |
|---------------------------------------|---------------|
| FCH_PCIE_RSTJ_GPP FOR APU PCIE DEVICE | PCIE 16X |
| PCIE_RST2J_GPP FOR FCH PCIE DEVICE | PCIE 1X / LAN |
| PCIE_ARSTJ FOR LPC DEVICES | SIO |

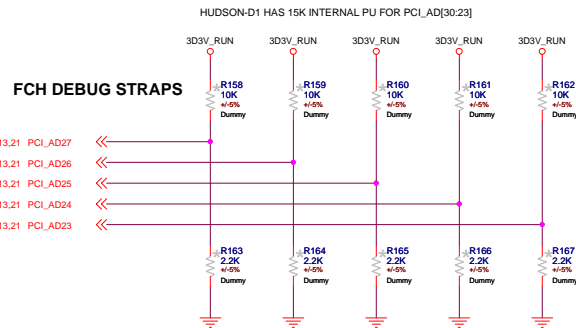


| | |
|------------------------|-------------------------------|
| USB_FSD1 Not connected | |
| USB_FSD0 Not connected | |
| USB13 | FRONT USB3.0 HEADER |
| USB12 | FRONT USB3.0 HEADER |
| USB11 | REAR USB3.0 connected |
| USB10 | REAR USB3.0 connected |
| USB9 | FRONT USB2.0 HEADER |
| USB8 | FRONT USB2.0 HEADER |
| USB7 | FRONT USB2.0 HEADER |
| USB6 | FRONT USB2.0 HEADER |
| USB5 | PS/2 USB DUAL STACK CONNECTOR |
| USB4 | PS/2 USB DUAL STACK CONNECTOR |
| USB3 | DUAL STACK CONNECTOR |
| USB2 | DUAL STACK CONNECTOR |
| USB1 | RJ45 DUAL STACK CONNECTOR |
| USB0 | RJ45 DUAL STACK CONNECTOR |





| | PCI_CLK1 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | RTC_CLK | GPIO199 |
|------------------|---------------------------------------|---|--|----------------------------------|-------------------------------------|-------------------------------|---------------------------------|
| PULL HIGH | ALLOW PCI E GEN2 | USE DEBIO STRAPS | NON-FUSION APU CLOCK MODE | EC ENABLED | CLKGEN ENABLED DEFAULT | SS+ DISABLE DEFAULT | ROM TYPE: H = LPC ROM |
| PULL LOW | FORCE PCI E GEN1 DEFAULT | IGNORE DEBIO STRAPS DEFAULT | FUSION APU CLOCK MODE DEFAULT | EC DISABLED DEFAULT | CLKGEN DISABLED | SS+ ENABLE | L = SPI ROM DEFAULT |



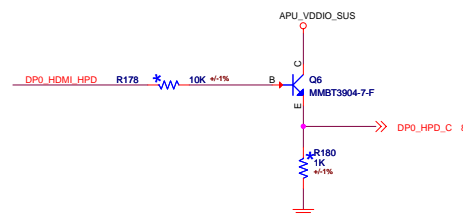
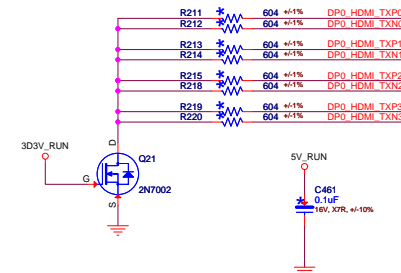
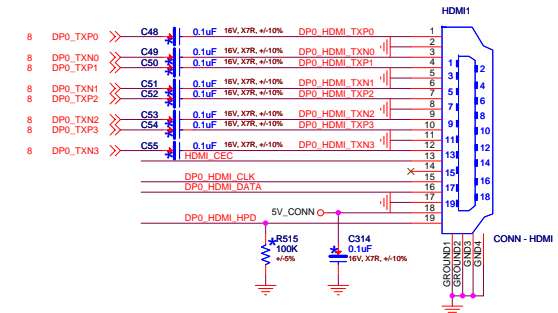
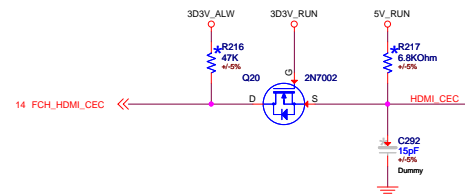
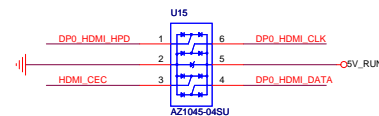
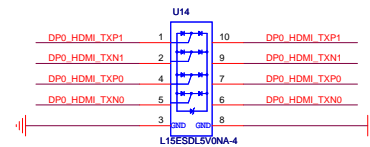
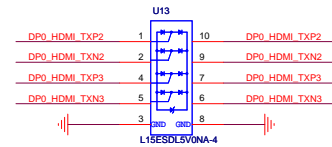
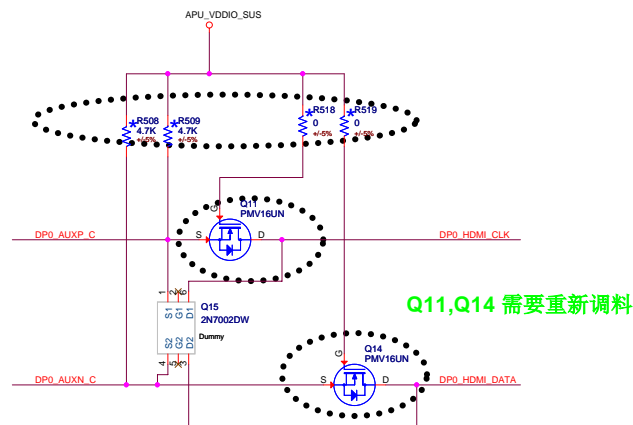
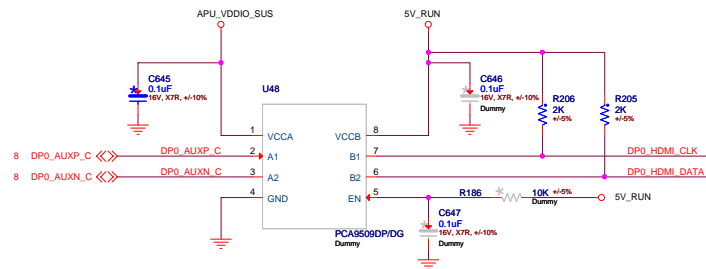
| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|------------------|----------------------------------|----------|--|---|---|
| PULL HIGH | USE PCI PLL DEFAULT | RESERVED | Normal REFCLK termination DEFAULT | USE DEFAULT PCI E STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | RESERVED | Inverted REFCLK termination | USE REPPROM PCI E STRAPS | ENABLE PCI MEM BOOT |



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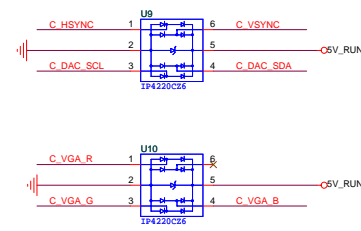
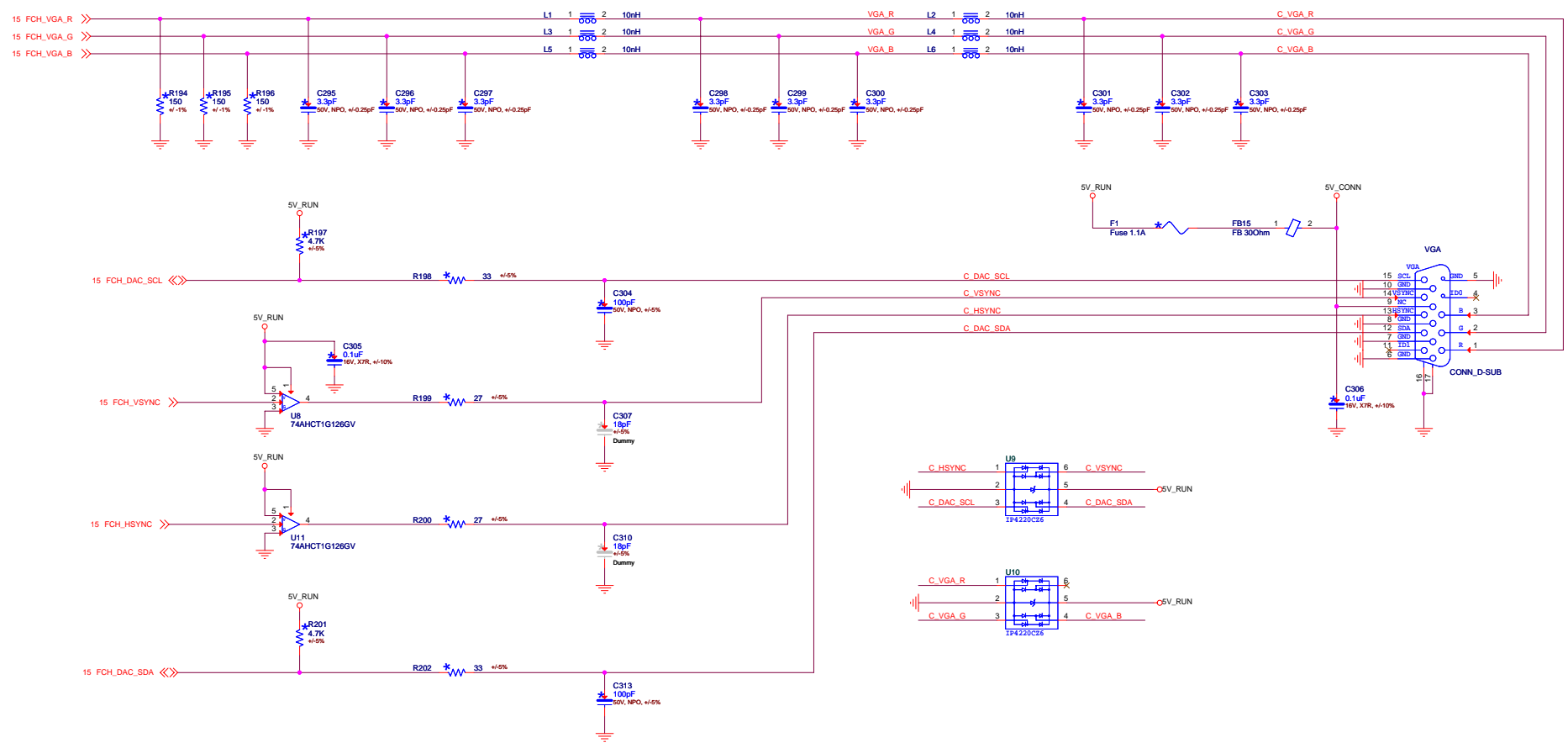
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| Title | | | FCH-STRAPS | |
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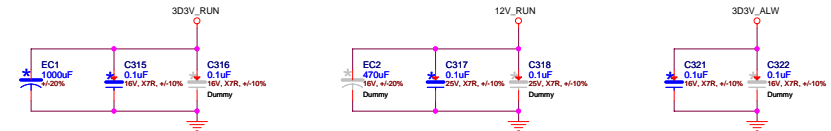
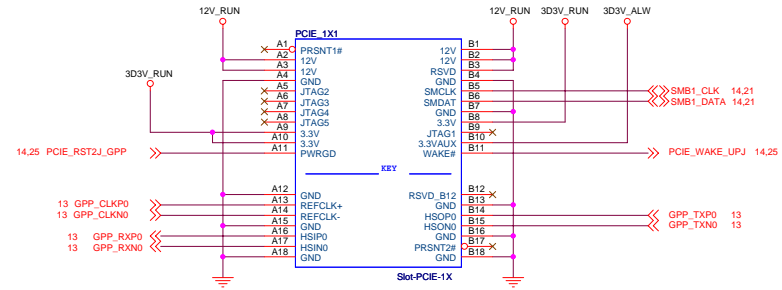
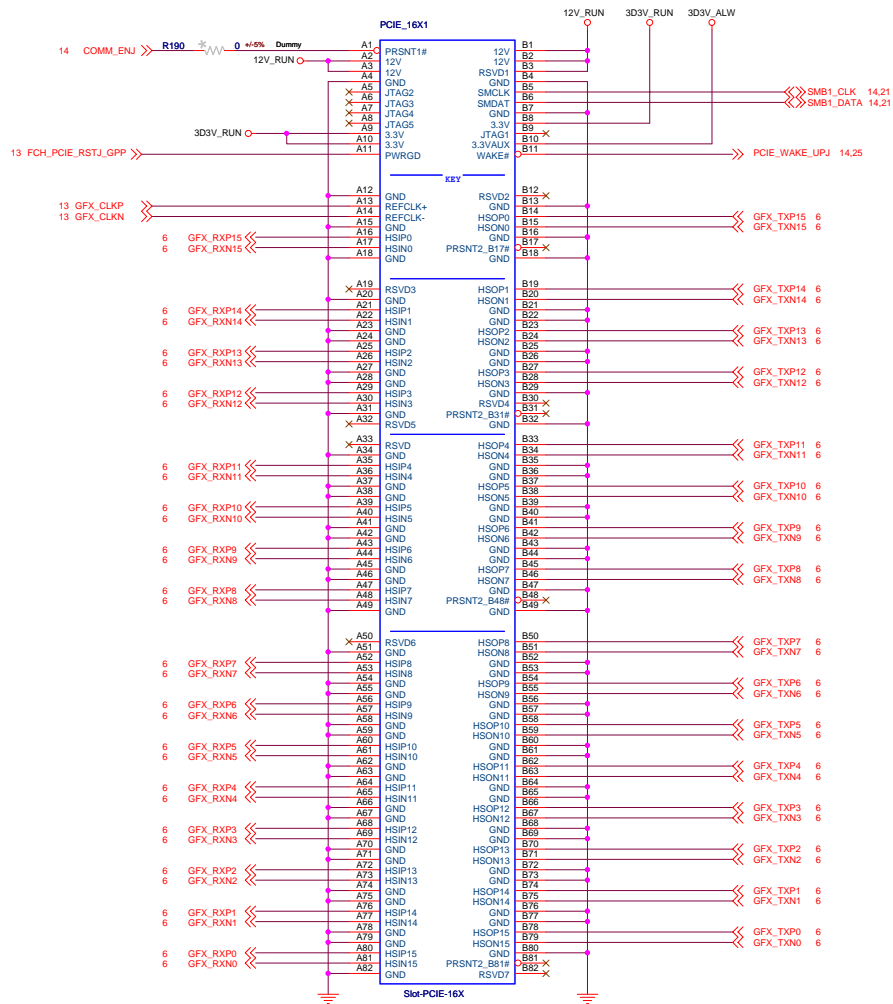
HDMI CONNECTOR



2011-09-01: For fix HDMI can't display issue

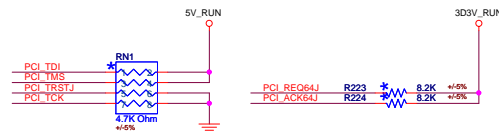
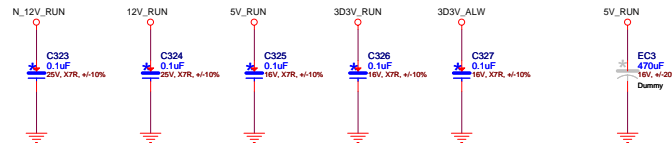
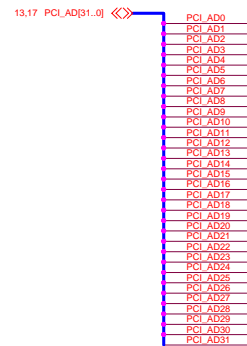
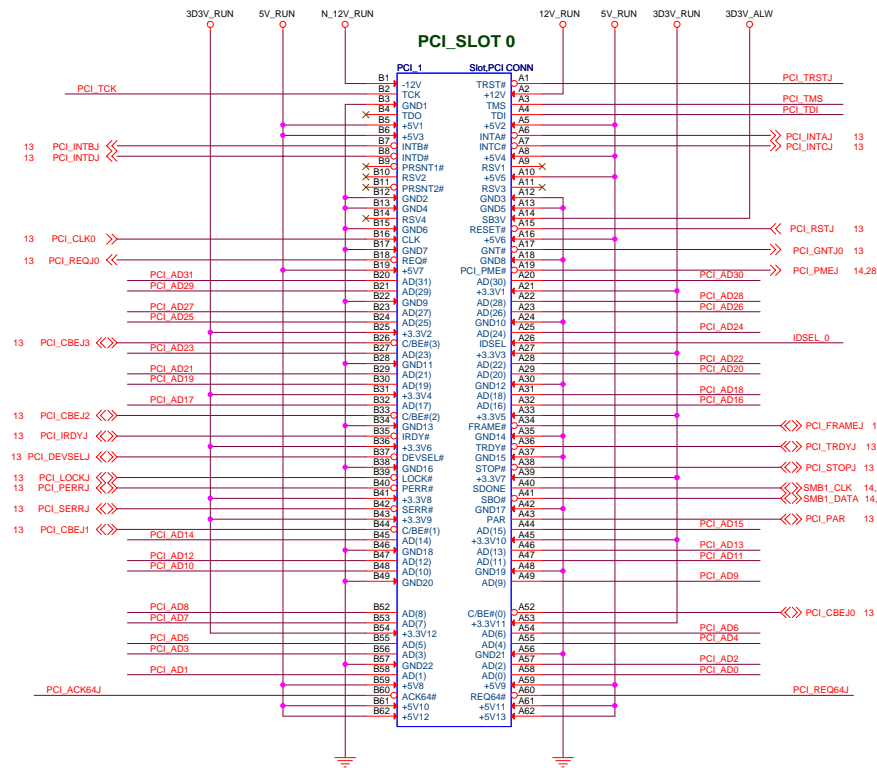
- 1, Change RN21 RESA from 1Kohm to R508,R509(4.7Kohm), R518,R519(0ohm)
2, Change Q11,Q14 from 3904 to PMV16UN





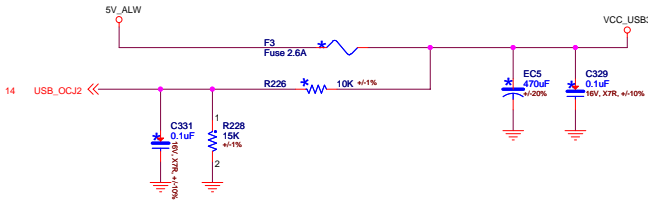
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|-------|-------------------------|-------|--------------------|
| Title | | | PCIE X16 & X1 SLOT |
| Size | Document Number | Rev | |
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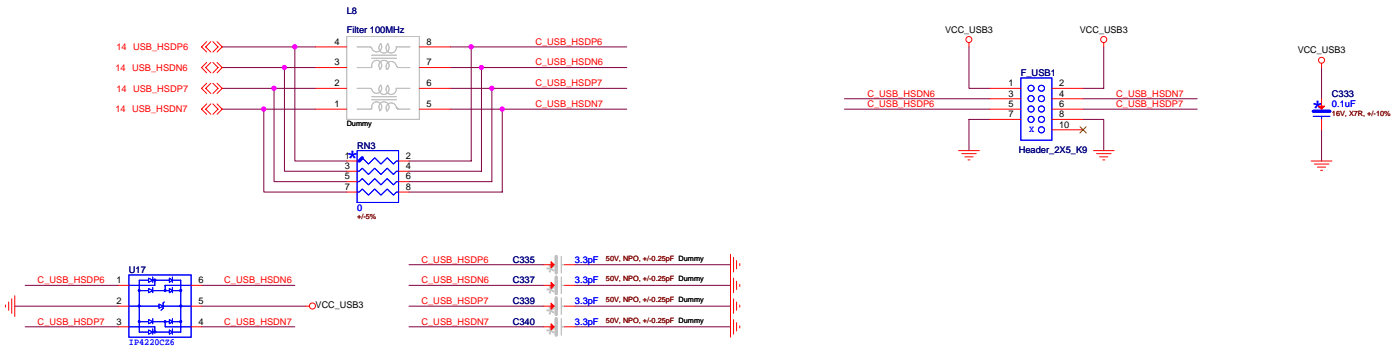


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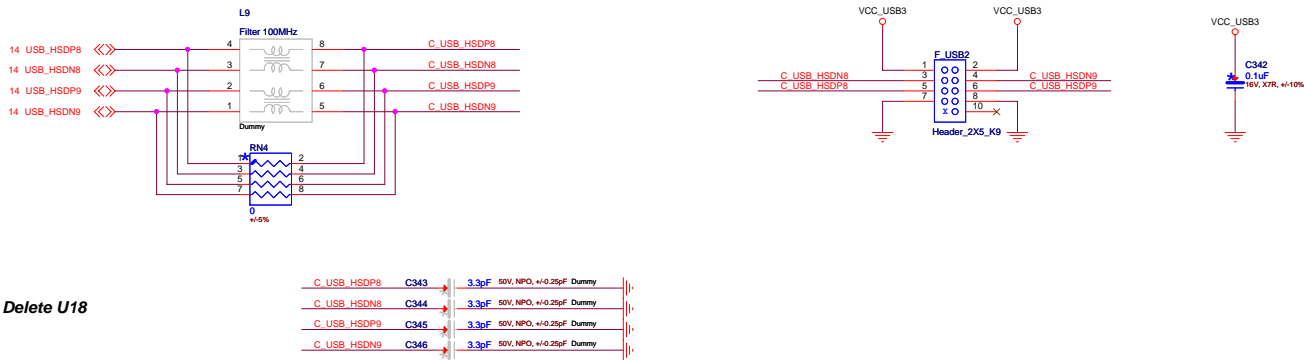
USB POWER(VCC_USB3) for FUSB1 & FUSB2



FUSB1 (Data 6 & 7)

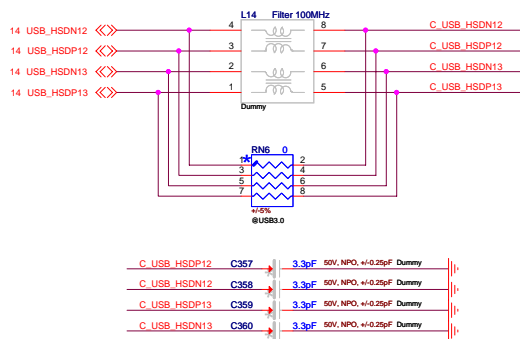
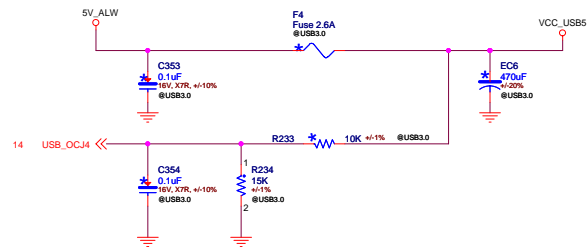


FUSB2 (Data 8 & 9)

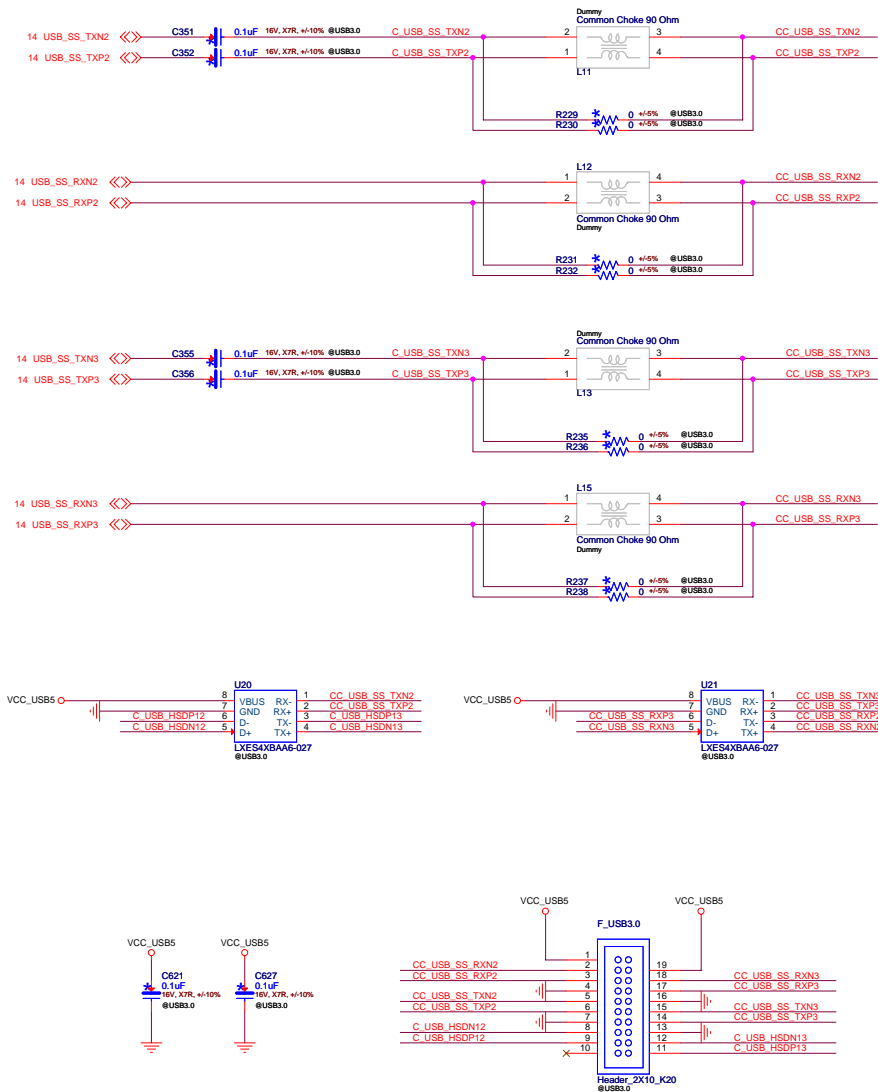


2011-07-27: Delete U18

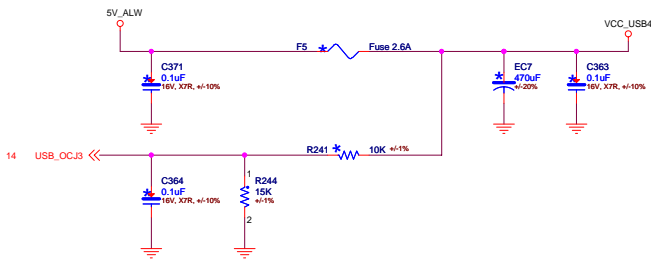
USB POWER (VCC_USB5) for FUSB3.0



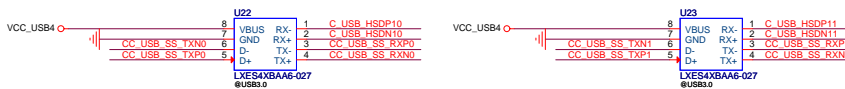
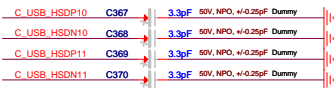
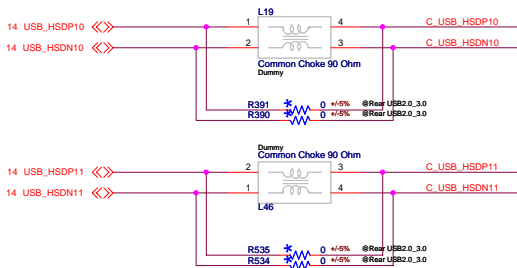
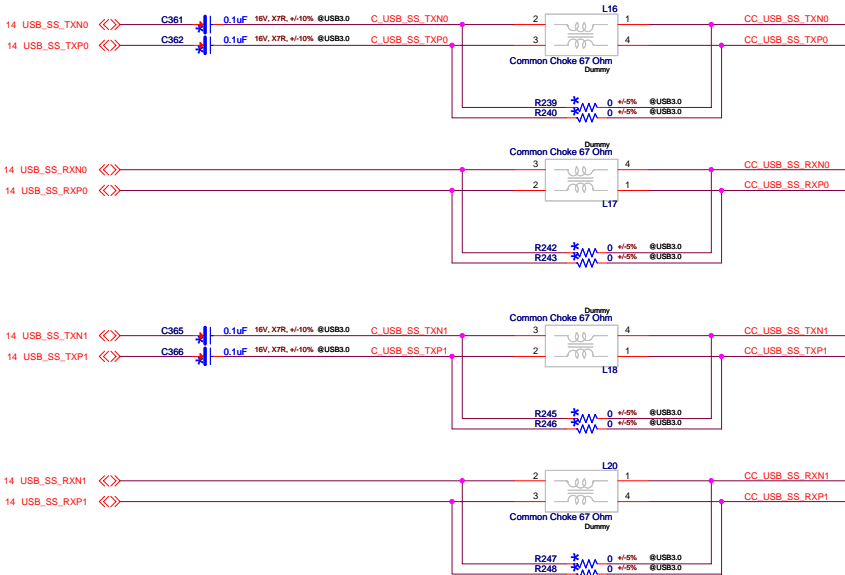
FUSB3.0 (USB3.0 data 2 & 3 / USB2.0 data 12 & 13)



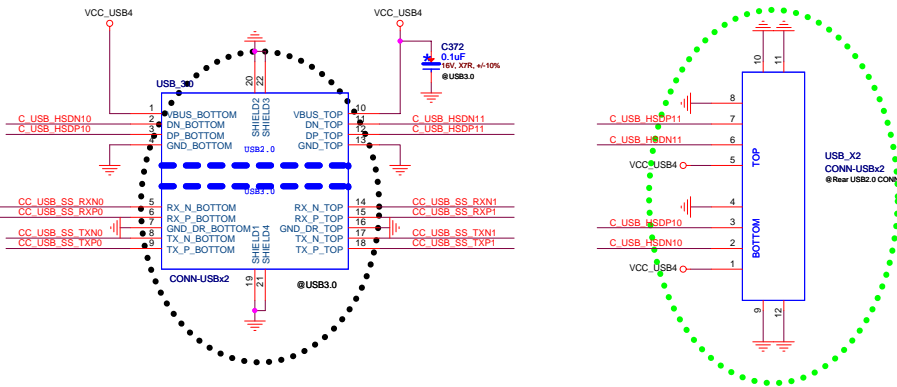
USB POWER (VCC_USB4) for USB3.0 & NIC_USB1



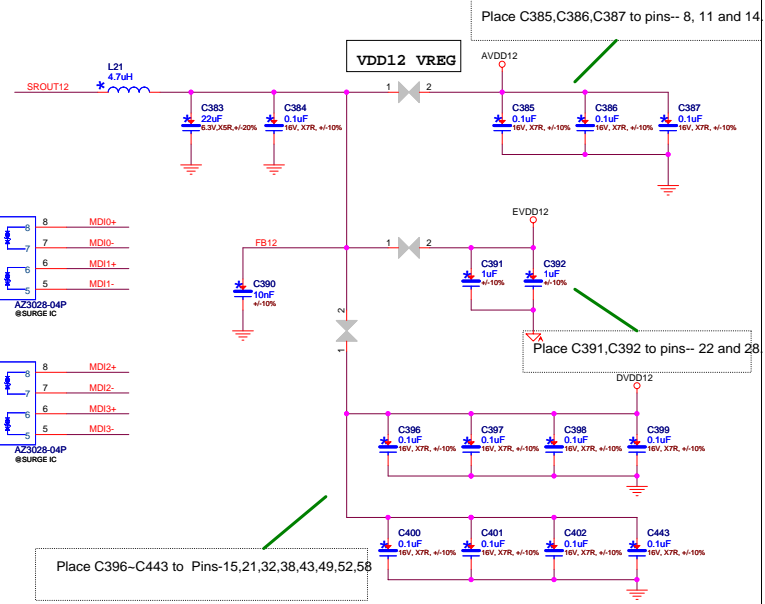
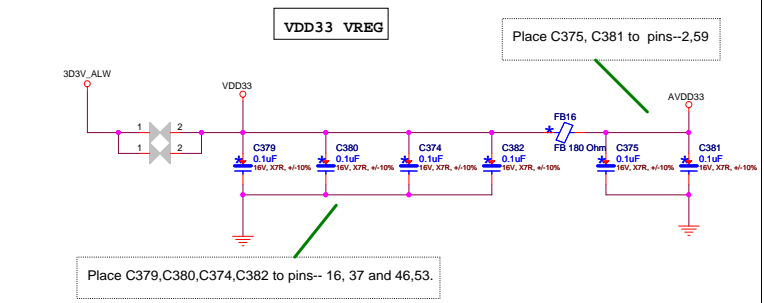
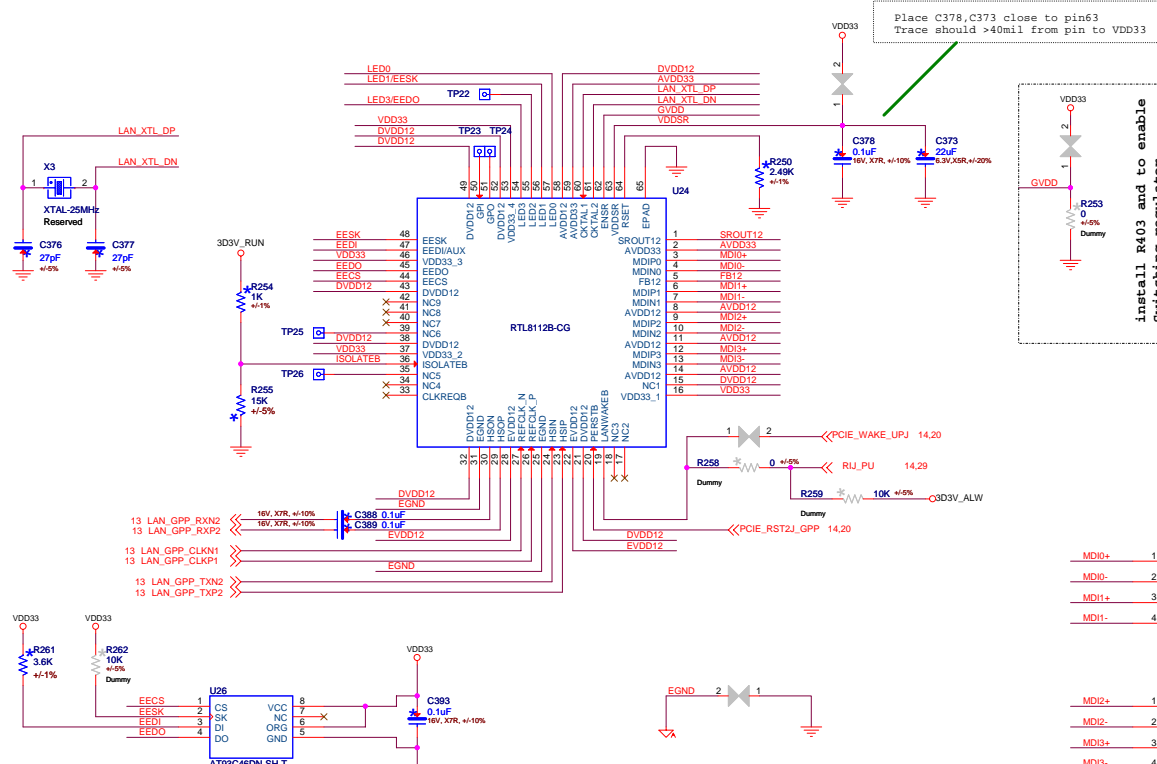
REAR USB3.0 (USB3.0 data 0 & 1 / USB2.0 data 10 & 11)



USB3.0 CONN CO-LAY USB2.0 CONN

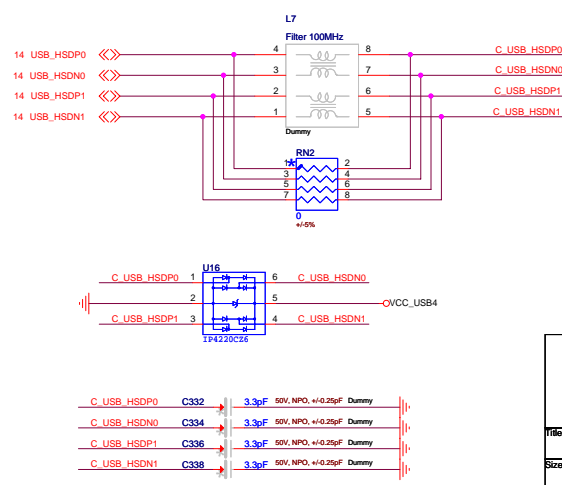
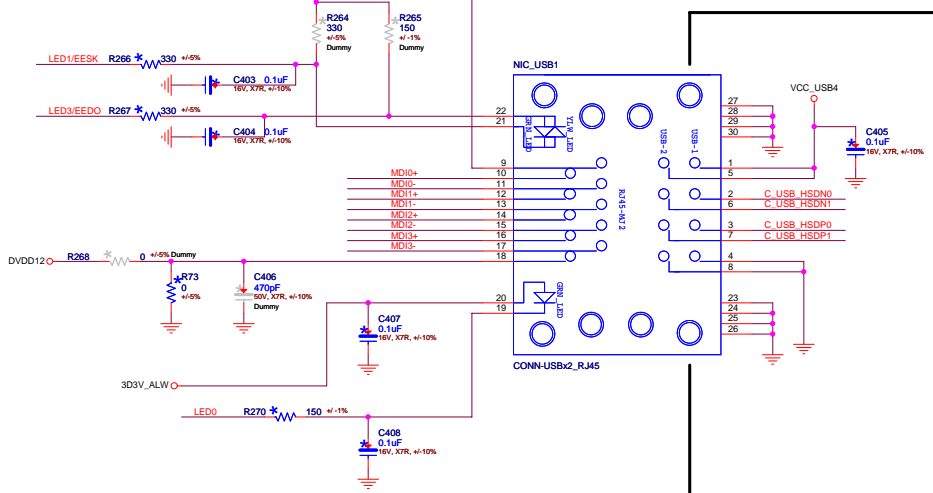


2011-08-31: Change USB3.0 CONN from 34041R400-600-G to 34041QY00-600-G(shorter)

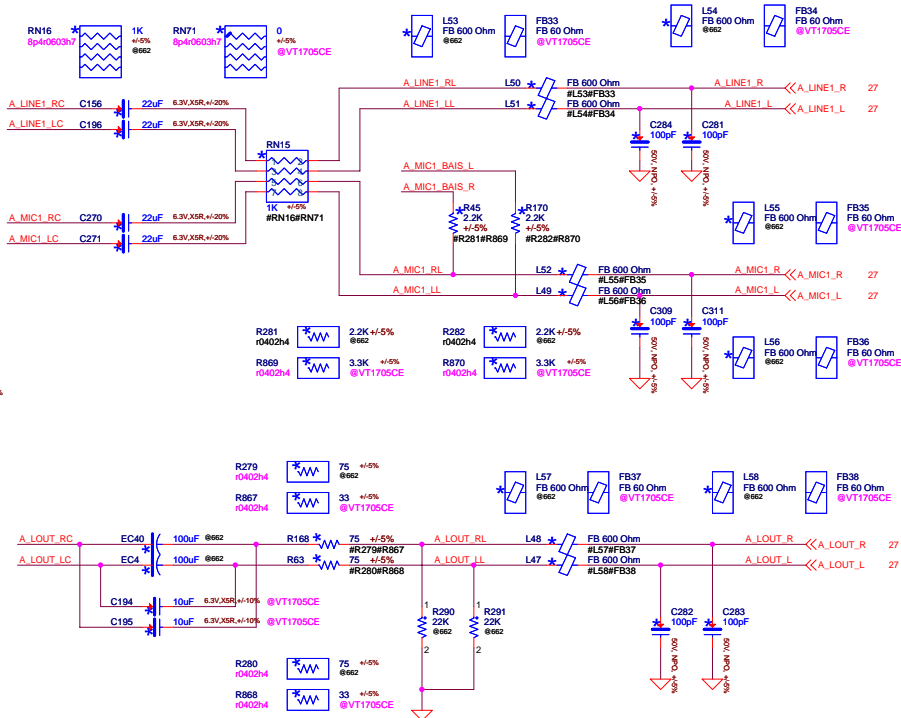


BACK PANEL (LAN + 2 USB Connector)

2 USB Connector



Colay



A LINE2_BIAS

3

2

1

4

5

DUMMY

BATS4A

R225 4.7K Dummy A LINE2_R

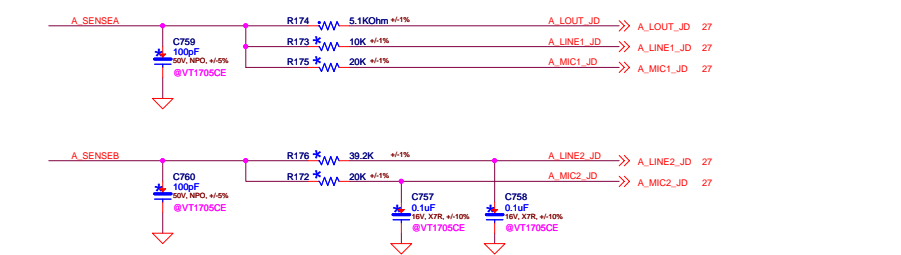
R193 4.7K Dummy A LINE2_L

R225, R193 FOR ALC662

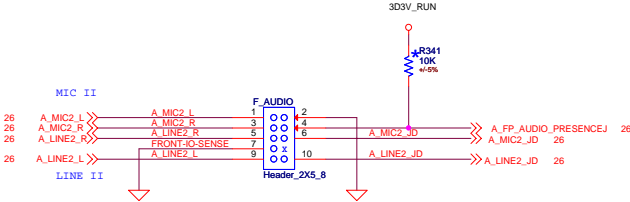
R328 3.3K ∇ -5% Dummy A LINE2_RL

R227 3.3K ∇ -5% Dummy A LINE2_LL

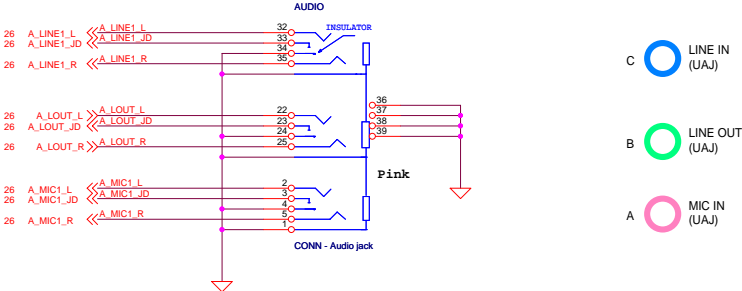
R328, R227 FOR VT1705CE



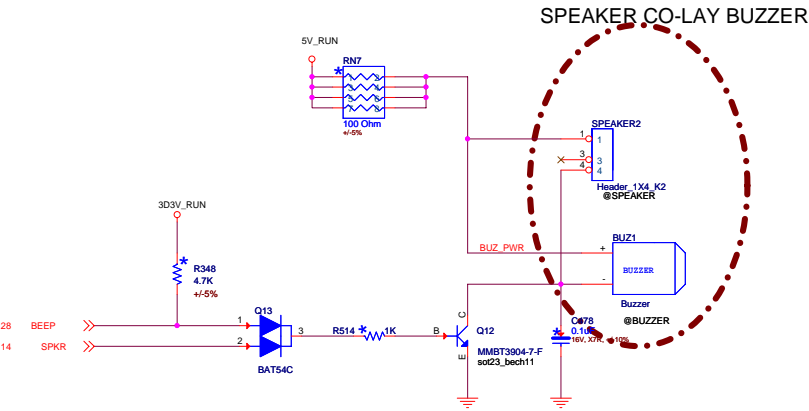
Front_Audio



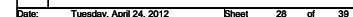
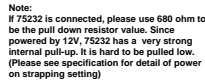
3 PORT Audio Jack

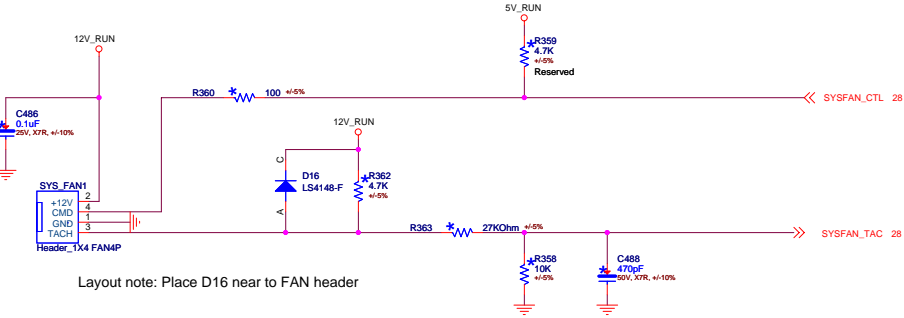
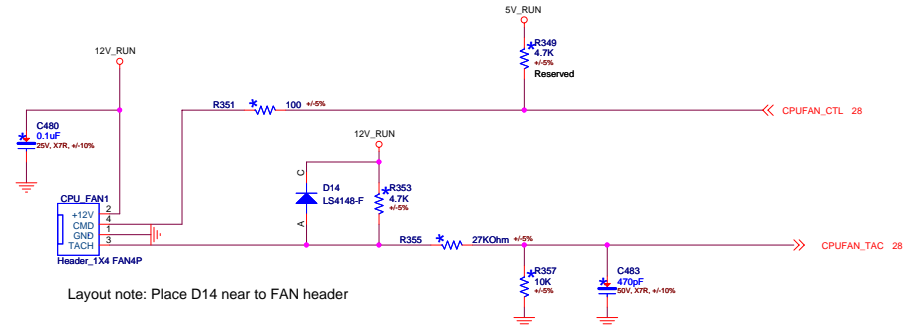


BUZZER/Speaker Header

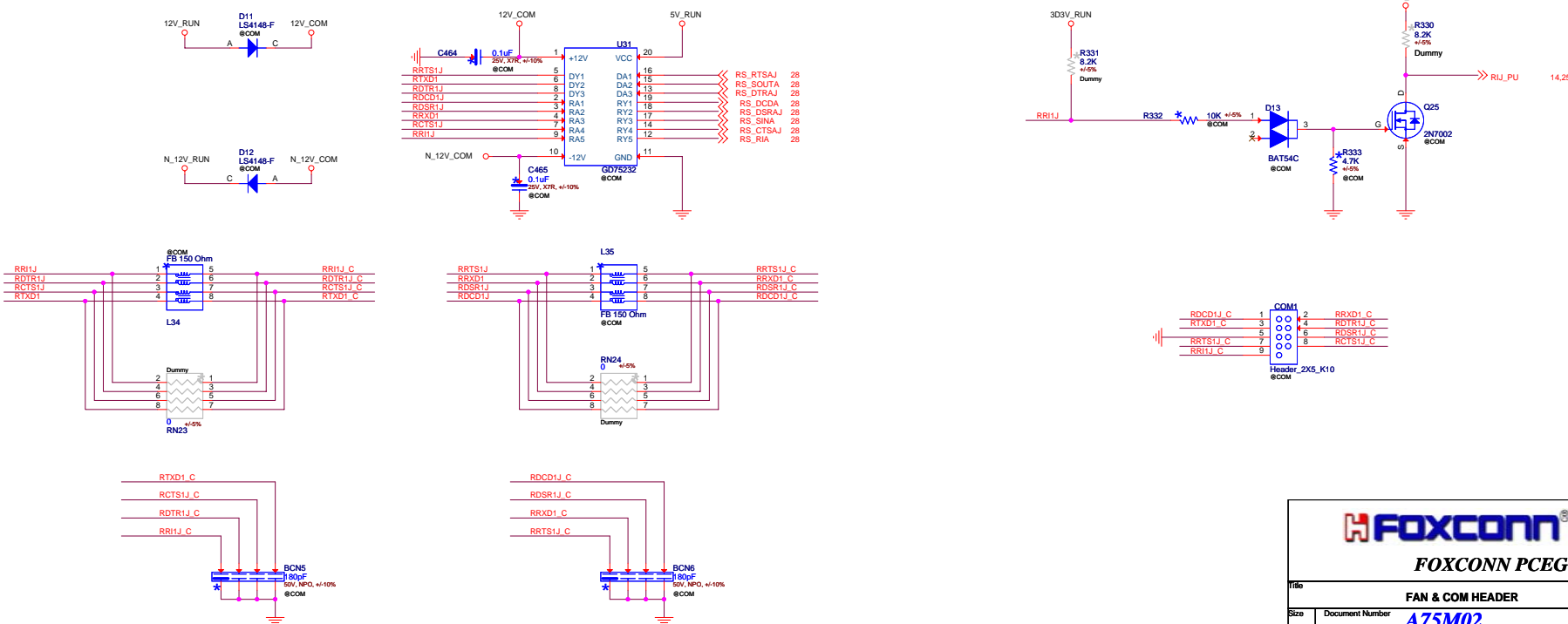


| | Symbol | Strapping Event | value | Description |
|----------------------------|-------------|----------------------------|-------|--|
| JP2 (Pin 57) | WDT_EN | internal VCC-OK LRESET# | 1 | Disable WDT to reset PWRGD |
| | | | 0 | Enable WDT to reset PWRGD |
| JP4 (Pin 61) | K8PWR_EN | internal VCC-OK | 1 | Disable K8 power sequence function |
| | | | 0 | Enable K8 power sequence function |
| | | | 11 | The default value of EC index 63h/6Bh/73h is 80h |
| JP3 & JP5 (Pin59&Pin21) | FAN_CTL_SEL | internal VCC-OK | 10 | The default value of EC index 63h/6Bh/73h is FFh |
| | | | 01 | The default value of EC index 63h/6Bh/73h is 00h |
| | | | 00 | The default value of EC index 63h/6Bh/73h is 40h |
| JP8 (Pin 30) | RSMRST_SEL | internal 3VSB_OK | 1 | RSMRST# output detected by 3VSB |
| | | | 0 | RSMRST# output detected by SYS_3VSB |

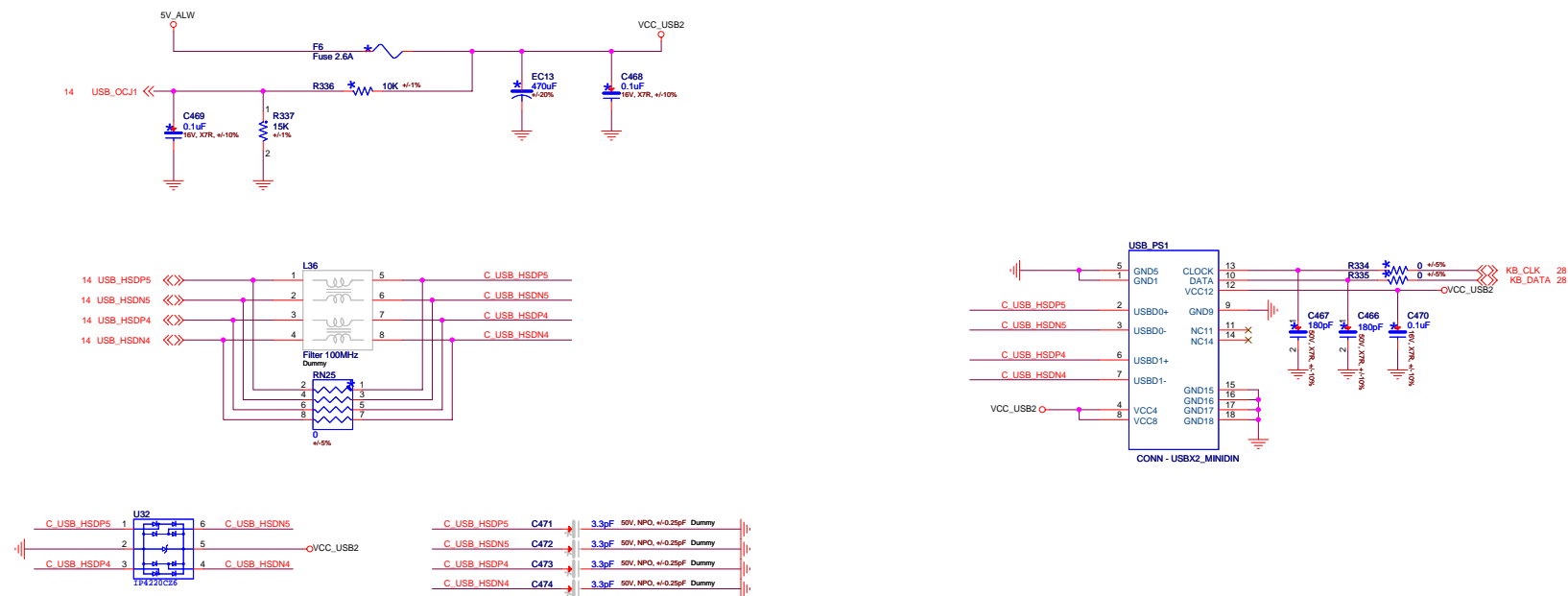




COM HEADER



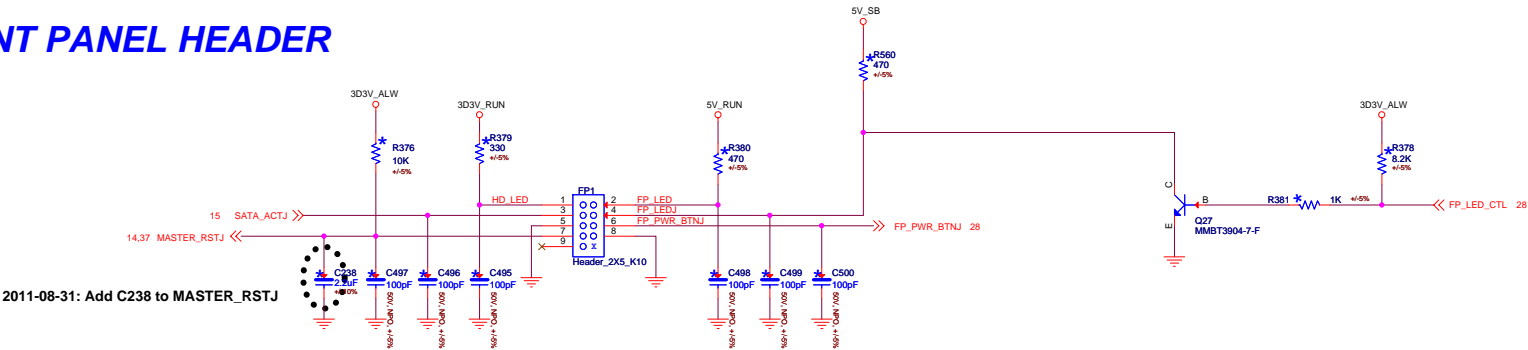
PS2_USB



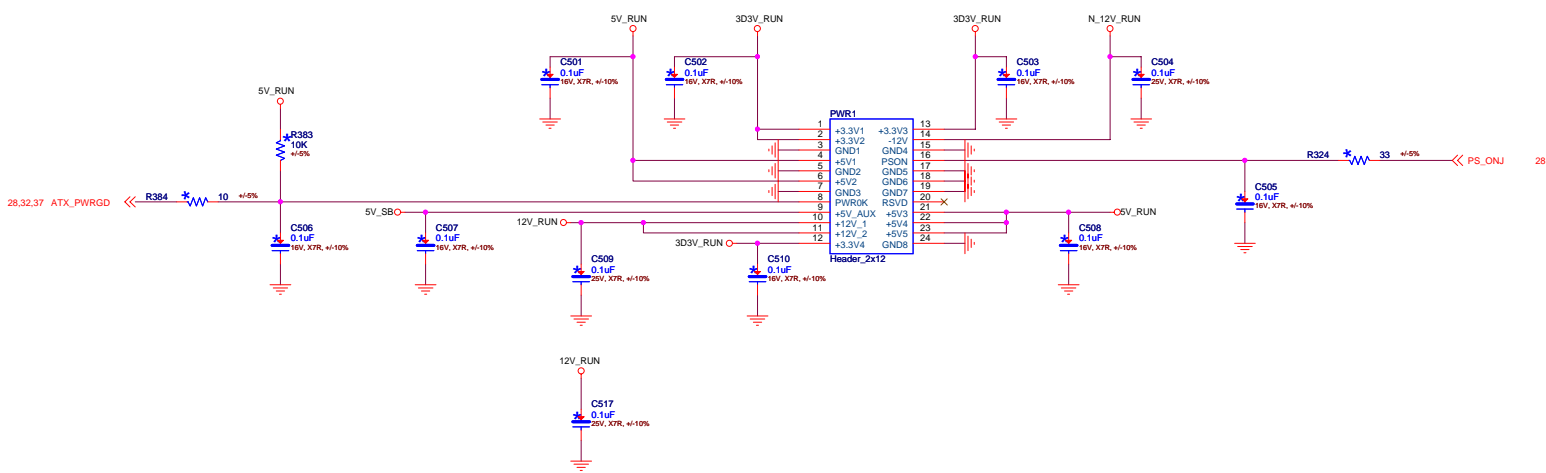
REAR_USB



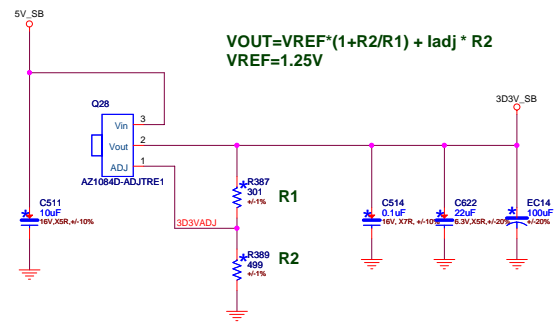
FRONT PANEL HEADER



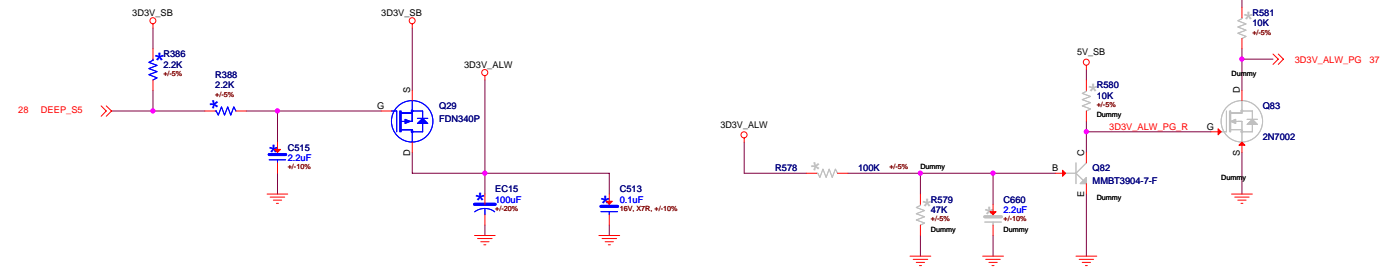
24 PIN ATX CONNECTOR



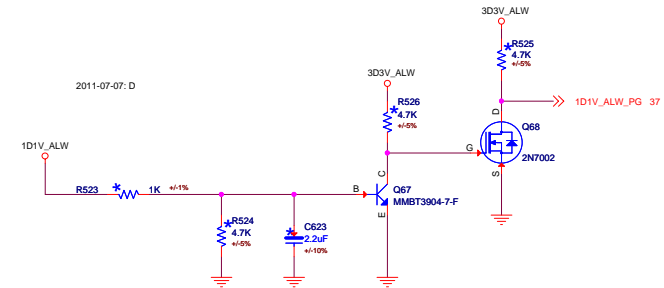
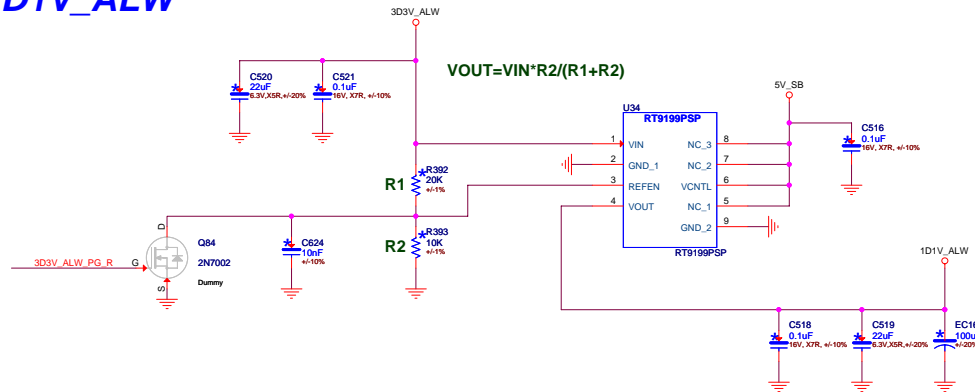
3D3V_SB



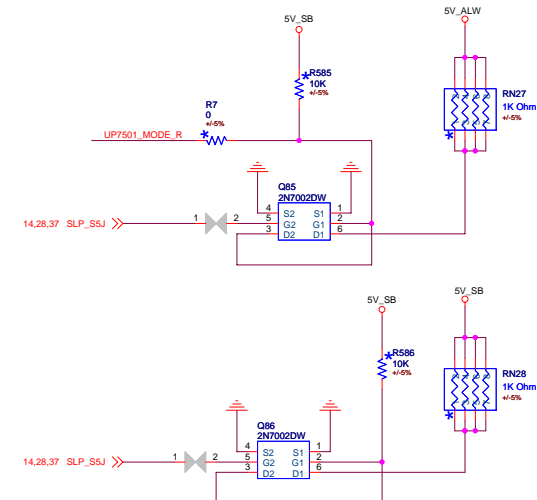
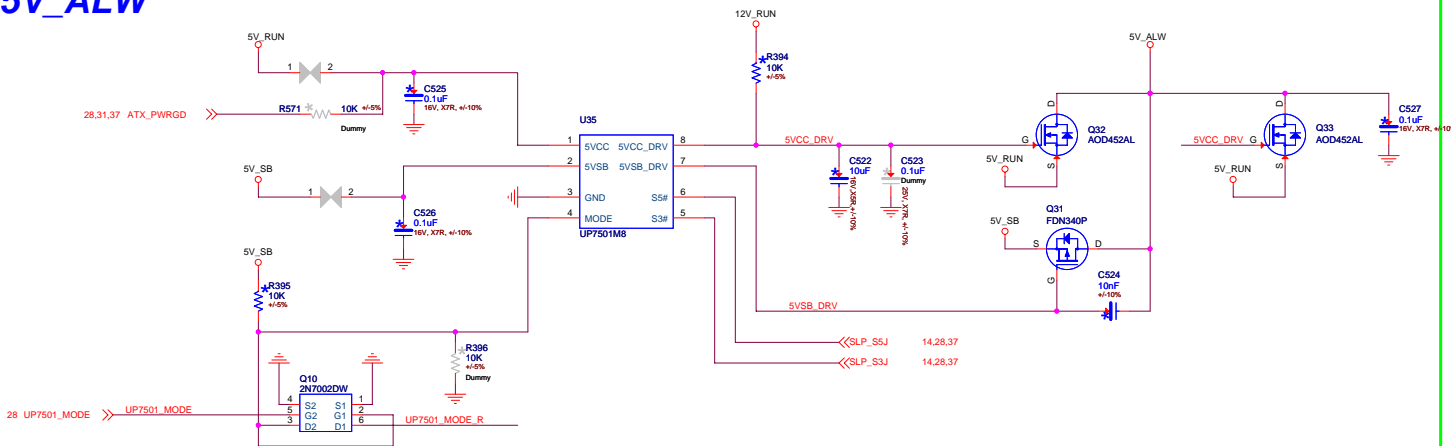
3D3V_ALW



1D1V_ALW



5V_ALW

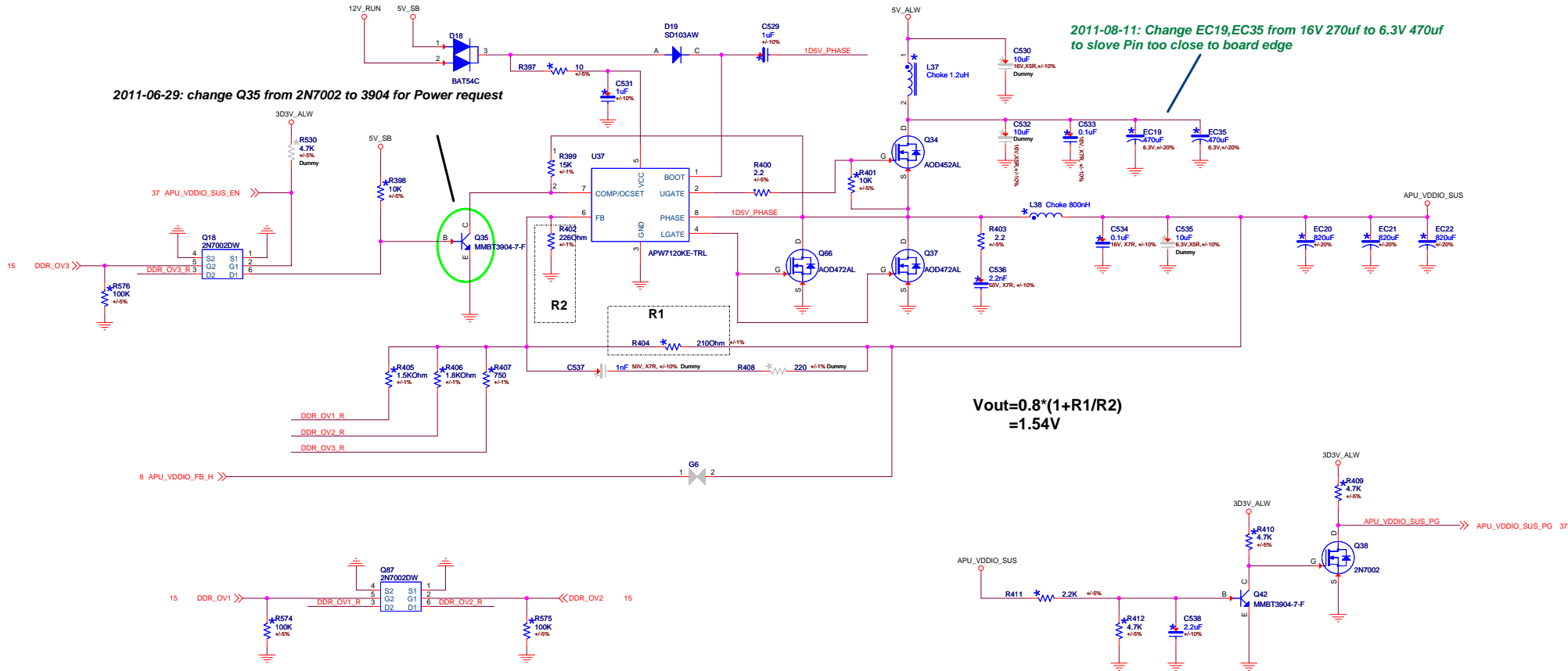


| S5# | S3# | MODE | 5V_ALW |
|-----|-----|------|----------|
| H | H | X | 5VCC |
| H | L | X | 5VSB |
| L | X | H | 5VSB |
| L | X | L | Shutdown |

FOXCONN

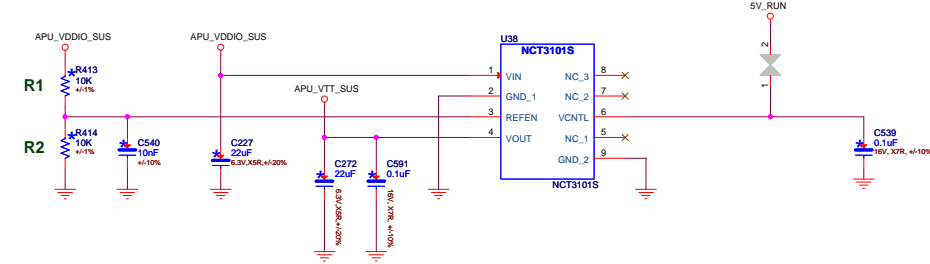
FOXCONN PCEG

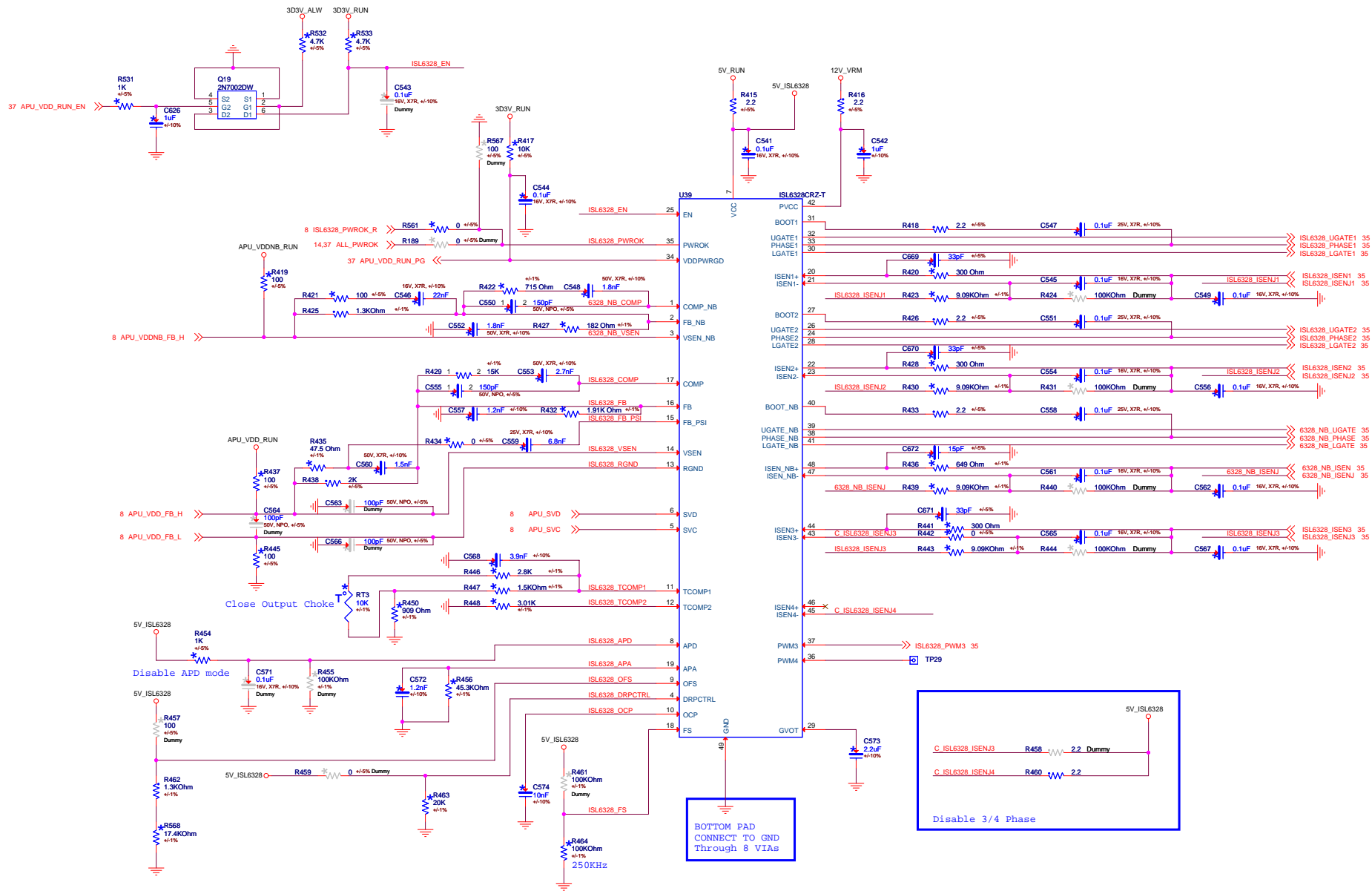
APU_VDDIO_SUS



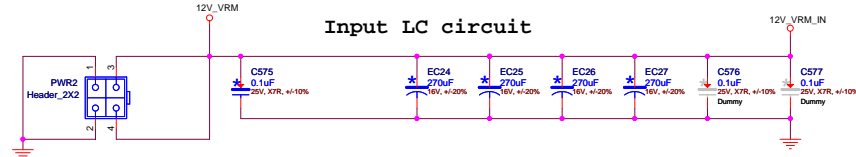
APU_VTT_SUS

$V_{OUT} = V_{IN} * R2 / (R1 + R2)$

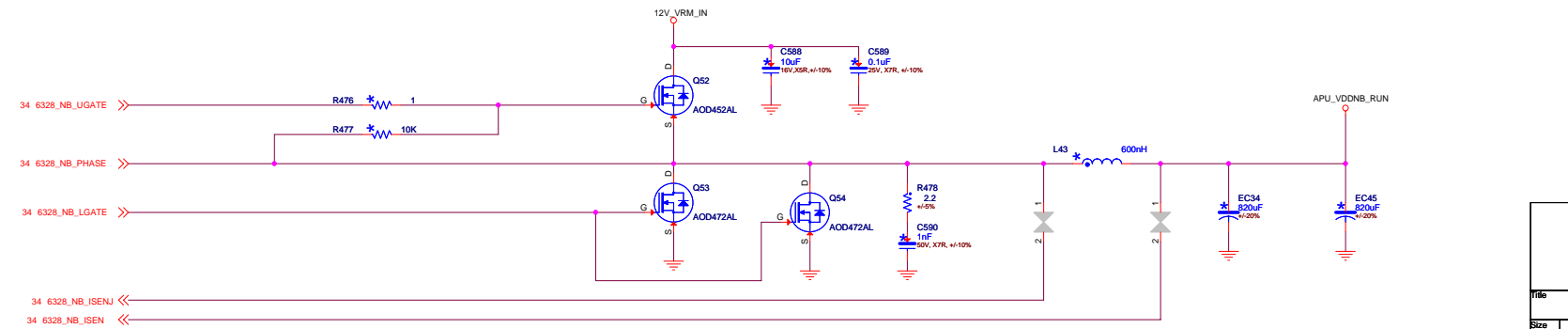
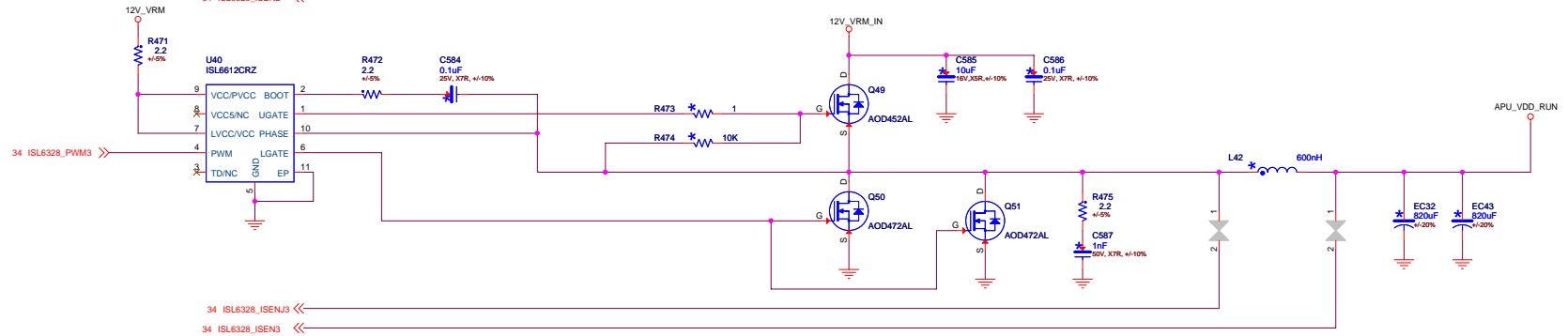
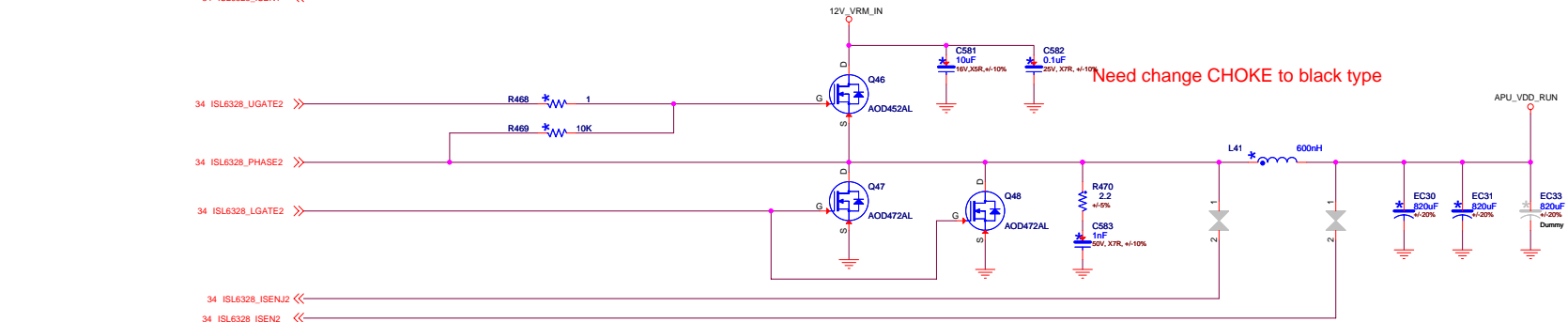
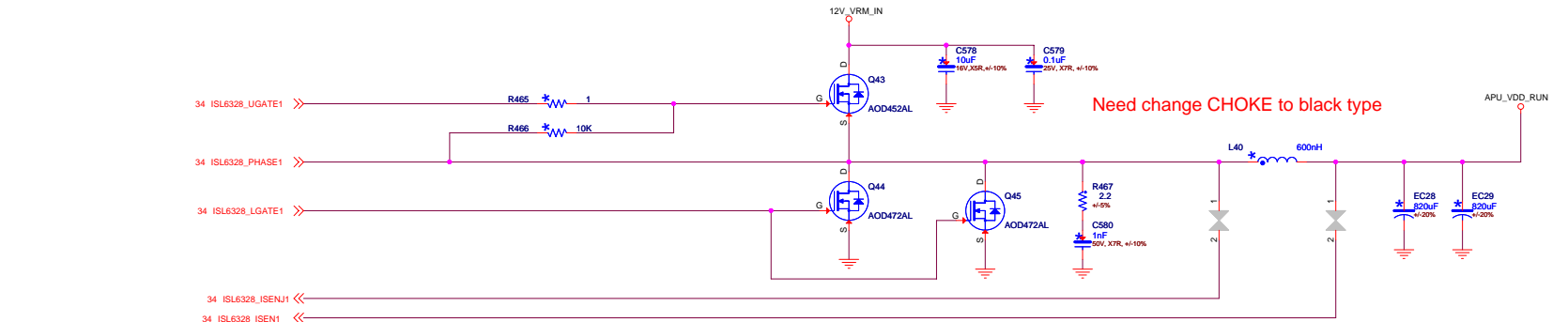




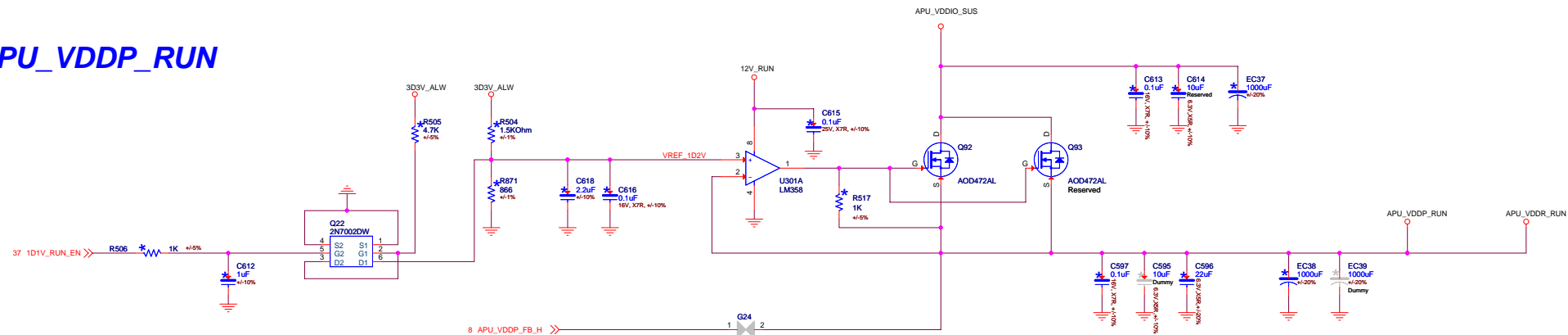
Input LC circuit



FOXCONN
FOXCONN PCEG

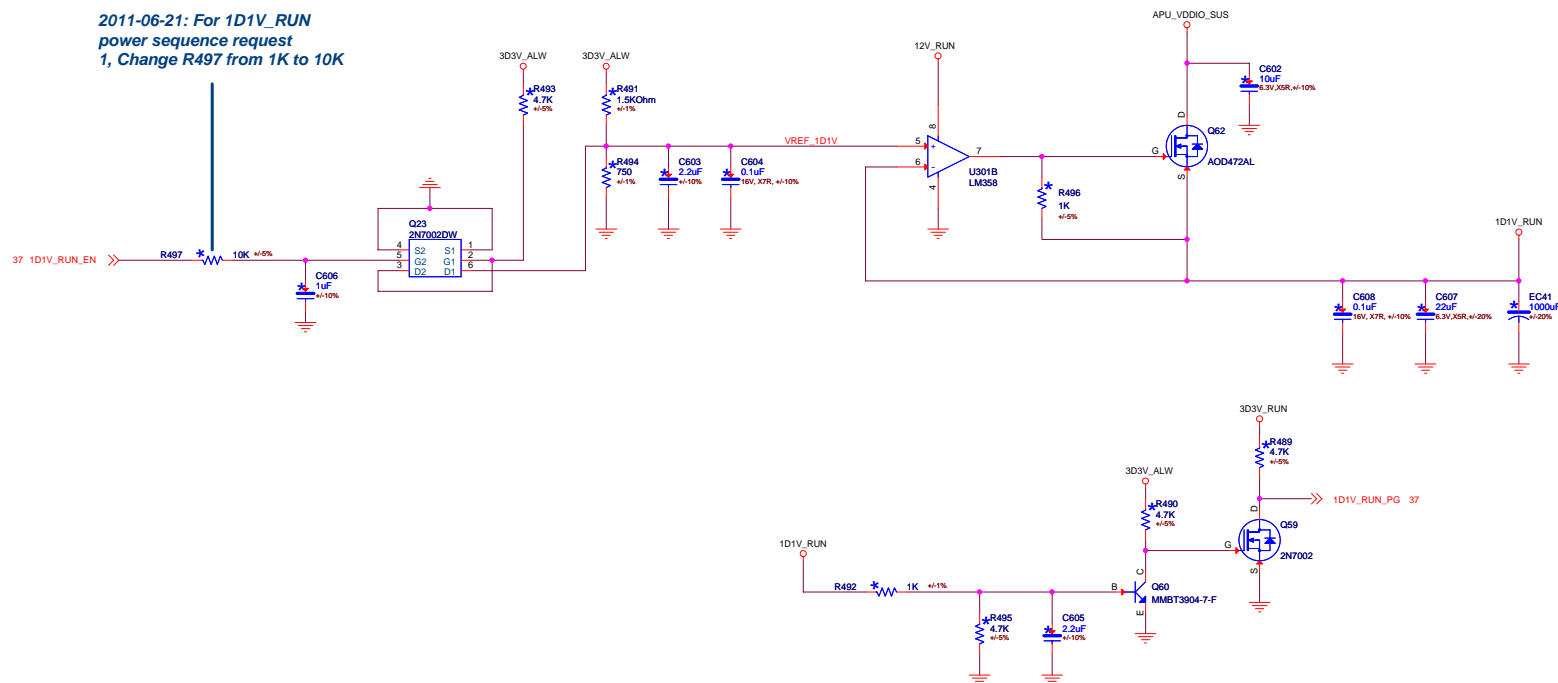


APU_VDDP_RUN

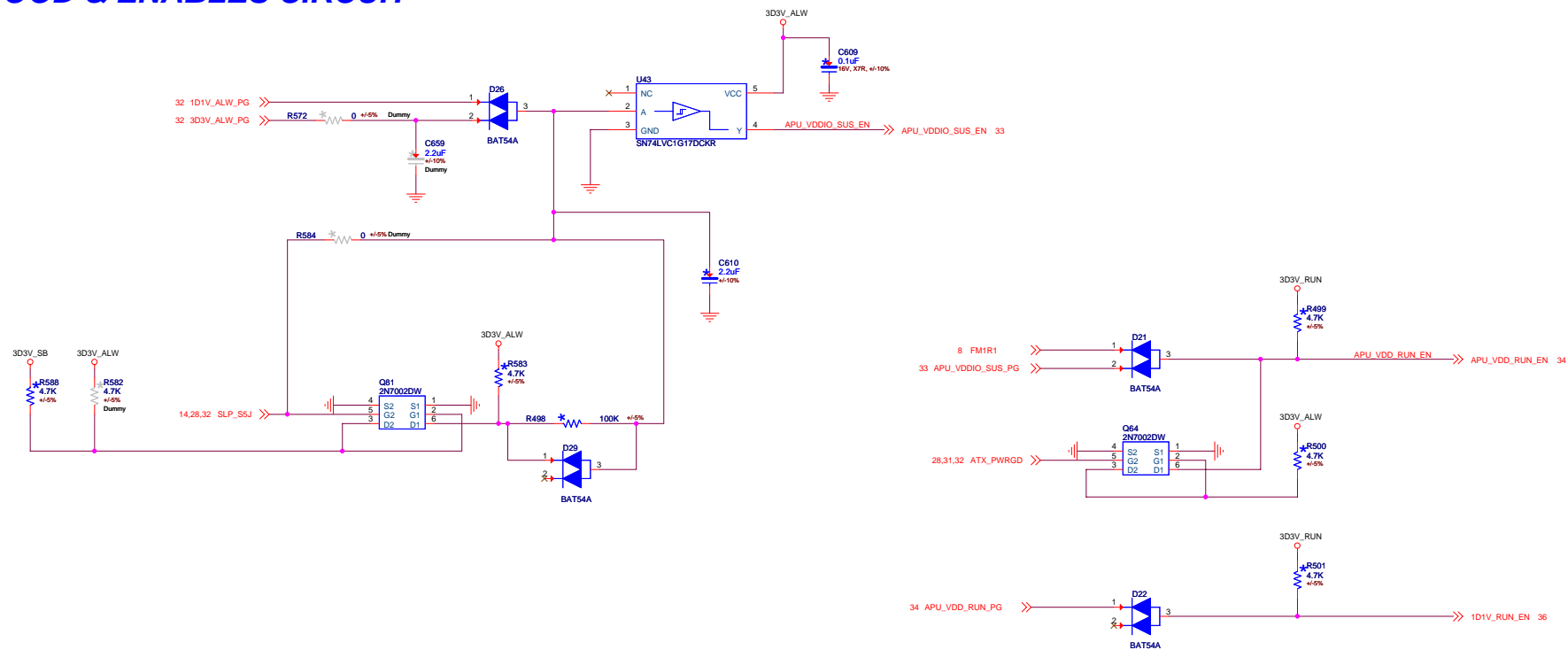


1D1V_RUN

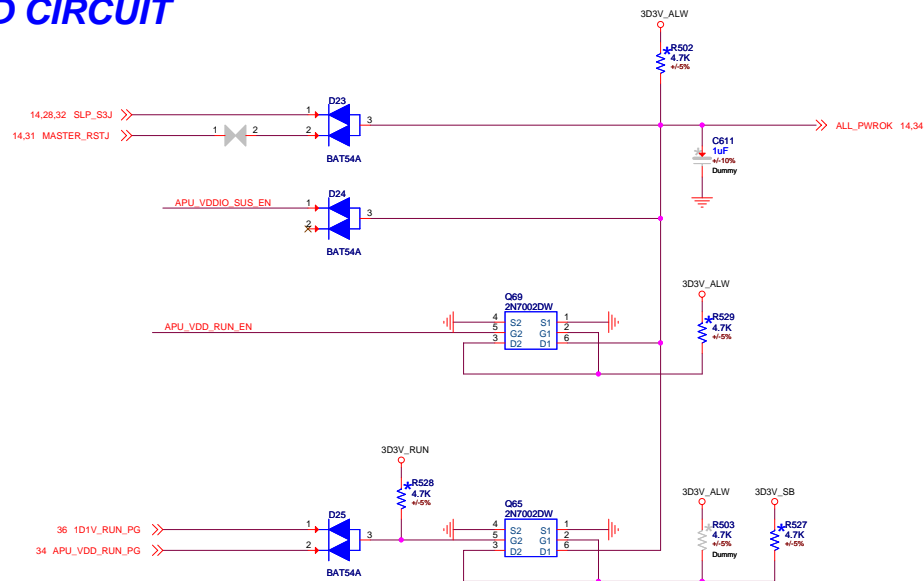
**2011-06-21: For 1D1V_RUN
power sequence request
1, Change R497 from 1K to 10K**

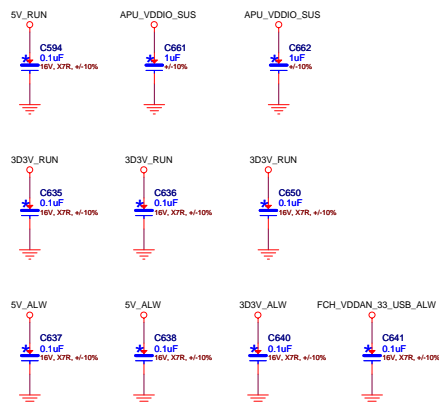
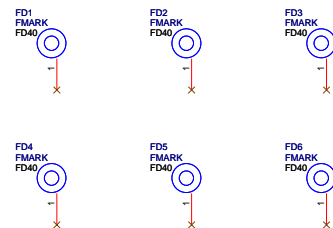
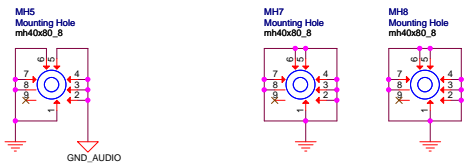
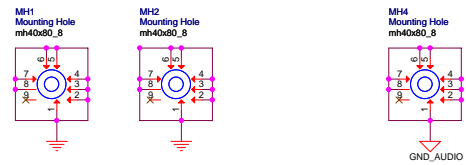


POWER GOOD & ENABLES CIRCUIT



ALL POWER GOOD CIRCUIT





FOXCONN PCEG

| | | | |
|---------------|-------------------------|-------|----------|
| Title | | | |
| EMC & MH & FD | | | |
| Size | Document Number | Rev | |
| | A75M02 | 1.0 | |
| Date: | Tuesday, April 24, 2012 | Sheet | 38 of 39 |

FAB A-FAB 1.0

2011-08-11

- 1, Change EC19,EC35 from 16V 270uf to 6.3V 470uf to slove Pin too close to board edge, and Dummy EC19 (270uF 16V SP-CAP \$0.072, 470uF 6.3V SP-CAP \$0.0654)
- 2, Change FB10 from FB to GAP for match ITE request
- 3, 2011-08-20: exchange SYSFAN_TAC and SYSFAN_CTL
- 4, 2011-08-20: Change R99 from 0 ohm to 10 ohm to fix can't power on or power on slowly issue

2011-08-31

- 5: Add C238 to MASTER_RSTJ
- 6: APU_VDDIO_SUS Dummy EC22
- 7: Change USB3.0 CONN from 34041R400-600-G to 34041QY00-600-G(shorter) (price is the same \$0.38)
- 8: Dummy R7,R585,Q85,RN27,Q86,RN28,R586

2011-09-01

- 2011-09-01: For fix HDMI can't display issue
 - 1, Change RN21 RESA from 1Kohm to R508,R509(4.7Kohm), R518,R519(0ohm)
 - 2, Change Q11,Q14 from 3904 to PMV16UN



FOXCONN PCEG

| | | |
|----------------|-------------------------|----------------|
| Title | | |
| CHANGE HISTORY | | |
| Size | Document Number | Rev |
| | A75M02 | 1.0 |
| Date: | Tuesday, April 24, 2012 | Sheet 39 of 39 |